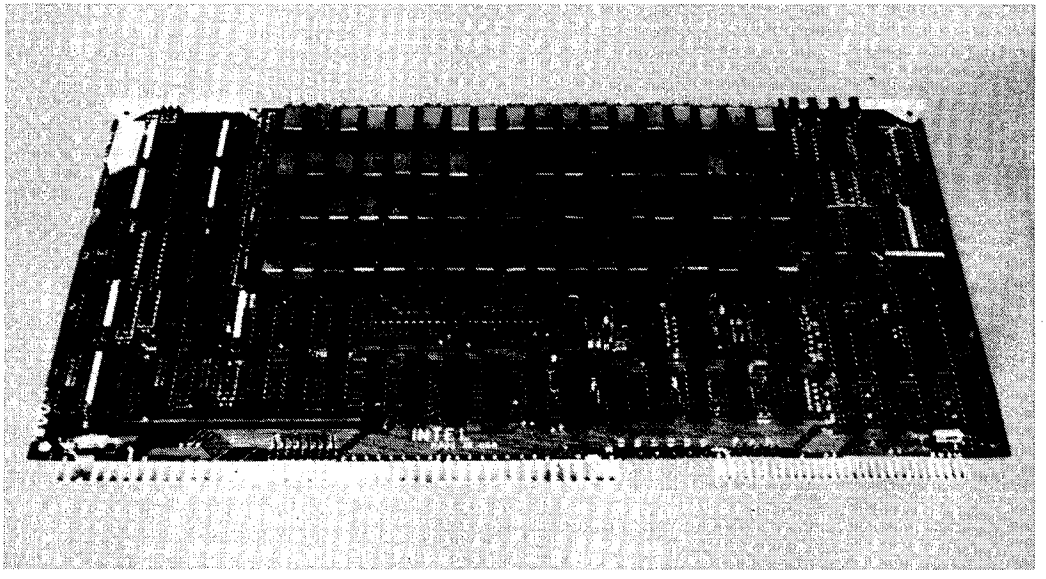
iSBC® 012B
RAM MEMORY BOARDS

- **iSBC® 86, iSBC 88 and iSBC 80 Board RAM Expansion Through Direct MULTIBUS® Interface**
- **512K of Read/Write Memory**
- **On-Board Parity Generator/Checker and Error Status Register**
- **Requires a Single +5V Power Supply**
- **Assignable Anywhere Within a 16 Megabyte Address Space**
- **Jumper Selectable Base Address on any 16K Byte Boundary**
- **Auxiliary Power Bus and Memory Protect Control Logic for Battery Backup RAM Requirements**

The iSBC 012 RAM memory board is a member of Intel's complete line of iSBC memory and I/O expansion boards. The board interfaces directly to any iSBC 86, iSBC 88 or iSBC 80 Single Board Computer via the MULTIBUS interface to expand system RAM capacity. The iSBC 012B board contains 512K bytes of read/write memory implemented using dynamic RAM components. An on-board dynamic RAM controller refreshes a portion of these components every 16 microseconds. Each refresh cycle utilizes memory for 550 nanoseconds (maximum).

The iSBC 012B board generates byte oriented parity during all write operations and performs parity checking during all read operations. When a parity error is detected, the board can generate an interrupt on the MULTIBUS interface. In addition, the row and bank of the RAM array containing the error are stored in a Parity Flag Register. This register is accessible as a MULTIBUS I/O port. An on-board LED also provides a visual indication that a parity error has occurred.



143876-1

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Order Number: 143876-001

SPECIFICATIONS

Word Size

8 bits and 16 bits

Memory Size

524,288 bytes (iSBC 012B)

Access Time

330 ns (worst case)
300 ns (typical)

Cycle Times (Worst Case)

Read: 500 ns max.
Write: 500 ns max.
Refresh: 550 ns max.

Interface

All address, data and command signals are TTL compatible.

Address Selection

Memory: Base address is jumper selectable on any 16K byte boundary in a 16 megabyte address space. On-board RAM cannot cross a 4 megabyte address boundary.

Parity Flag Register: The I/O address of the Parity Flag Register is jumper selectable to be between 00H to 0FH or 40H to 4FH.

Connector

Edge Connector: 86-pin double-sided PC edge connector with 0.156 in. contact centers.

Mating Connector: Viking 3KH43/9AMK12 or equivalent.

Auxiliary Power

An auxiliary power bus is provided to allow separate power to RAM array for systems requiring battery backup of read/write memory. Selection of this auxiliary RAM power bus is made via jumpers on the board.

Memory Protect

An active-low TTL compatible memory protect signal is brought out on the auxiliary connector which, when asserted, disables read/write access to RAM on the board. This input is provided for the protection of RAM contents during system power-down sequences.

Physical Characteristics

Width: 12.00 in. (30.48 cm)
Height: 6.75 in. (17.15 cm)
Depth: 0.50 in. (1.27 cm)
Weight: 14 oz. (397 gm)

Electrical Characteristics

D.C. POWER REQUIREMENTS

All configurations require only +5V ±5%.

Normal System Operation (max.)

4.8A (worst case)
3.46A (typical)

Auxiliary Power No RAM Access (max.)

1.35A (worst case)
0.88A (typical)

Environmental Characteristics

Operating Temperature: 0°C to +55°C
Relative Humidity: to 90% (without condensation)

Reference Manual

143865-001— iSBC 056B/012B Hardware Reference Manual (not supplied)

Manuals may be ordered from any Intel sales representative, distributor office, or from Intel Literature Dept., 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 012B	512K-Byte RAM Board with Parity