iSBC 88/25™
SINGLE BOARD COMPUTER
HARDWARE REFERENCE MANUAL

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PREFACE

This manual provides general information, installation and setup instructions, programming guidelines for the on-board, programmable devices, board level principles of operation, and service information for the iSBC 88/25 Single Board Computer. Related information is provided in the following publications:

- *The iAPX 88 Book*, Order Number 210200.
- *iSBC Applications Manual*, Order Number 142687.
- *Intel Multibus Specification*, Order No. 9800683.
- *Intel Multibus Interfacing*, Application Note AP-28A.
- *Intel iSBX Bus Specification*, Order No. 142686.
- *Designing iSBX Multimodule Boards*, Application Note AP-96.
- *iSBC 337 Numeric Data Processor Hardware Reference Manual*, Order No. 142887.
- *iRMX 88 Reference Manual*, Order No. 143232.
- *Introduction to the iRMX 80/88 Real-Time Multitasking Executives*, Order No. 143238.
- *iRMX 88 Installation Instructions*, Order No. 143231.
- *iRMX 80/88 Interactive Configuration Utilities*, Order No. 142603.
- *Guide to Writing Device Drivers for the iRMX 86 and iRMX 88 I/O Systems*, Order No. 142926.
- *The Intel Peripheral Design Handbook.*
- *The Intel Component Data Catalog.*
- *The Intel Systems Data Catalog.*

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ILLUSTRATIONS

CHAPTER 1
GENERAL INFORMATION

1-1. INTRODUCTION

The iSBC 88/25 Single Board Computer is an Intel Multibus and iSBX Multimodule compatible, 8-bit computer system on a single printed circuit assembly (Figure 1-1). The iSBC 88/25 board includes an Intel 8088 microprocessor operating at 5 MHz, 4K bytes of on-board static random access memory (RAM), 24 programmable parallel I/O lines, one serial I/O port, three programmable interval timers and a programmable interrupt controller. Sockets are provided for a maximum of 64K bytes of read-only memory (ROM). The iSBC 88/25 board will also accept the iSBC 337 Numeric Data Processor Multimodule board.

On board RAM expansion may be accomplished in two increments, by first adding the iSBC 302 RAM Expansion Module, adding 8K bytes, for a total of 12K bytes. Then two additional 2168 RAM devices may be added to the iSBC 302 board for a total of 16K bytes.

The iSBC 88/25 board will also accept the JEDEC compatible so called "byte wide" RAM devices such as the Intel 2188 (8K x 8) dynamic RAMs. These "byte wide" RAMs reside in sockets normally used for ROM/EPROM devices and do not require any special refresh circuitry. Two of these devices may reside on-board, and four additional devices may be used with the iSBC 341 ROM Expansion Module.

On-board ROM size may be increased by adding the ROM/EPROM device which suits your application. The four on-board sockets will accept either 24-pin or 28-pin ROM/EPROM devices such as Intel 2716 (2K x 8), 2732 (4K x 8), 2764 (8K x 8) and 27840 (16K x 8) devices to a maximum of 64K bytes of ROM/EPROM on-board. In addition, on-board ROM/EPROM size may be increased to a maximum of 128K bytes, using the iSBC 341 ROM Expansion Module.

Alternatively, the iSBC 88/25 board and the iSBC 341 ROM Expansion board may be equipped with Intel 2854 Electrically Erasable Programmable Read-Only Memory (EEPROM) devices. These devices allow on-board reprogramming using iSBC 88/25 board circuitry and an external power source.

Additional on-board I/O capabilities are provided via the two iSBX Multimodule connectors on the iSBC 88/25 board. These connectors allow any of the optional 8-bit iSBX Multimodule boards to be used on the iSBC 88/25 board.

The Intel 8088 microprocessor is software compatible with the Intel 8086 microprocessor. The iSBC 88/25 board will operate with the Intel iRMX 88 or the iRMX 86 Realtime Multitasking Executive operating system.

This hardware reference manual provides the information you will need to promptly install and operate

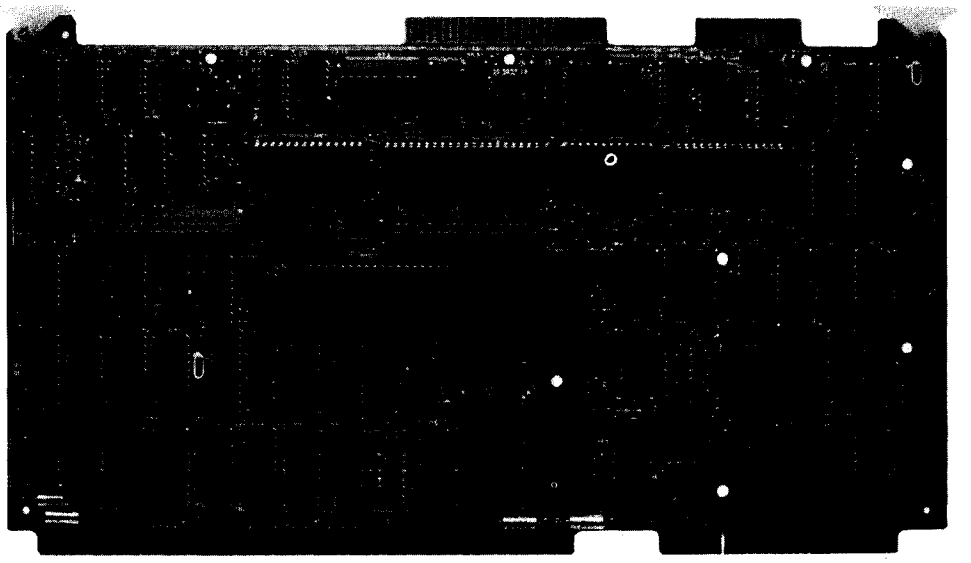


Figure 1-1. iSBC 88/25Single Board Computer

the iSBC 88/25 Single Board Computer. To optimize your application of this board, we suggest reading the entire manual before attempting installation and operation.

1-2. DESCRIPTION

The iSBC 88/25 board is controlled by an Intel 8088 microprocessor operating at 5 MHz. Processor support is provided by an Intel 8284A Clock Generator-Driver and an Intel 8288 Bus Controller.

Up to 1 Megabyte of total system memory can be directly addressed by the iSBC 88/25 board. Of this amount, a maximum of 144K bytes may reside on-board (16K RAM + 128K ROM). However if using the so called "byte wide" 28-pin RAM devices in ROM/EPROM sockets, RAM size will increase, and ROM/EPROM size will decrease accordingly.

The iSBC 88/25 board is shipped from the factory with the two Intel 2168 RAM devices in sockets U51 and U67. These two devices provide 4K bytes of on-board RAM. To increase the amount of on-board RAM beyond 4K bytes, the optional iSBC 302 RAM expansion module must be installed. The RAM expansion module is equipped with four Intel 2168 devices, thereby adding 8K bytes of on-board RAM. This results in a total of 12K bytes of on on-board RAM.

The iSBC 302 RAM Expansion Module plugs directly into socket U52 and U68. Two additional 2168 RAM devices may be installed on the iSBC 302 RAM Expansion Module, for a maximum of 16K bytes. The last two devices occupy the highest RAM address space (see Table 2-2 for RAM addressing). Installing any additional RAM requires a jumper installation.

In addition, the so called "byte wide" 28-pin RAM devices may be used on the iSBC 88/25 board, residing in two on-board ROM/EPROM sockets and up to four iSBC 341 sockets.

The board will accept a wide variety of Intel programmable read-only memory devices. Either 24 or 28-pin devices may be used. Four on-board sockets are provided, with expansion provided by the optional iSBC 341 ROM Expansion Module. Refer to Chapter 2 for complete information.

The on-board 8253-5 Programmable Interval Timer provides three independent counter outputs which may be configured to a variety of applications, including frequency output, rate generator, interval timer and real-time interrupts. One of the counters serves as the baud rate clock for the on-board 8251A Programmable Communications Interface device.

Serial I/O operation is handled by an Intel 8251A Programmable Communications Interface device. The board is configured to the RS 232C standard. However, this may be converted to a current loop TTY serial interface using optional equipment. Baud rates are software programmable using the on-board interval timer.

The iSBC 88/25 board utilizes one Intel 8255A-5 Programmable Peripheral Interface device to control the three, 8-bit, parallel I/O ports. All 24 lines may be configured to a variety of dedicated or general purpose applications. One port is equipped with an Intel 8287 Bus Transceiver. The other two ports are equipped with sockets for line drivers or terminators.

All interrupts, except the Intel 8088 non-maskable interrupt (NMI), are handled by the on-board Intel 8259A Programmable Interrupt Controller device. System interrupts can be connected to the interrupt controller via the Multibus lines, and additional interrupts may originate from one or two iSBX Multimodule boards. An on-board interrupt jumper matrix allows interrupt configuration flexibility and provides priority selection.

Two iSBX bus connectors (J3 and J4) are provided on the iSBC 88/25 board. These connectors are designed to expand the board's I/O functions and add peripherals, using special purpose optional iSBX Multimodule boards, such as the iSBX 350 Parallel I/O Multimodule Board. The Multimodule boards reside directly on the iSBC 88/25 board. One or two iSBX Multimodules may be added, as required by your application.

Off-board system access is provided by the Multibus connector (P1) and an auxiliary connector (P2). Off-board peripheral operations are handled through 24 parallel I/O lines (connector J1), a serial communications channel (connector J2), and two iSBX Multimodule connectors.

The iSBC 88/25 board is designed to operate as a full bus master in any Intel Multibus compatible chassis or backplane. The board may also reside in your own custom chassis, using Multibus compatible connectors (refer to Chapter 2).

For enhanced numerics processing capability, the iSBC 337 Numeric Data Processor Multimodule extends the 8088 architecture and data set. Over 60 numeric instructions offer arithmetic, trigonometric, transcendental, and exponential high-speed operations. Supported data types with the iSBC 337 option include 16, 32, and 64-bit integer, and 32 and 64-bit floating point, 18-digit packed BCD and 80-bit temporary.

1-3. DOCUMENTATION SUPPLIED

Each iSBC 88/25 board is shipped with a corresponding set of schematic diagrams. These drawings

should be inserted into the back of this manual for future reference. Refer to Chapter 5 for related information.

1-4. ADDITIONAL EQUIPMENT REQUIRED

The iSBC 88/25 board requires few optional components for basic operation. Depending on your application, you may need to purchase a parallel I/O connector, a serial I/O connector, and additional RAM if more than 4K bytes are required. Any on-board ROM must also be purchased separately. Chapter 2 provides information for selecting these items.

1-5. SPECIFICATIONS

Specifications of the iSBC 88/25 board are provided in Table 1-1.

Table 1-1. Board Specifications

[redacted]	Intel 8088
[redacted]	[redacted]
Single Processor Cycle	200 nanoseconds
Minimum Processor Bus Cycle (four single cycles)	800 nanoseconds
MULTIBUS CLOCK	9.830 MHz (BCLK/ & CCLK/)
PCI Clock Input	2.458 MHz
PIT Input 0 & 2	1.229 MHz
PIT Input 1	153.6 KHz
RAM ACCESS TIME	100 nsecs max, Address to Data
ROM/PROM/EPROM ACCESS TIME	520 - 1120 nsecs (0 - 3 Waits)
MEMORY CAPACITY	1M Byte
Maximum On-Board ROM/EPROM	128K Bytes
Maximum On-Board RAM	16K Bytes
Remaining Off-Board Expansion	856K Bytes
[redacted]	[redacted]
[redacted]	[redacted]
On-Board RAM, w/two 2168 + iSBC 302, partial	0 — 02FFF
On-Board RAM, w/two 2168 + iSBC 302, full	0 — 03FFF
On-Board ROM	FE000 — FFFFF using 2716 devices
	FC000 — FFFFF using 2732 devices
	F8000 — FFFFF using 2764 devices
	F0000 — FFFFF using 27840 devices
With iSBC 341 Expansion	FC000 — FFFFF using 2716 devices
	F8000 — FFFFF using 2732 devices
	F0000 — FFFFF using 2764 devices
	E0000 — FFFFF using 27840 devices
[redacted] **	All notation in hexadecimal
[redacted]	80 — 9F*
[redacted]	A0 - BF*
[redacted]	
[redacted] (OCW1)	C0
[redacted]	C2
[redacted]	
[redacted]	C8 - read/write
[redacted]	CA -
[redacted] Status	CC -
[redacted]	CE - write command
[redacted]	
[redacted]	D0
[redacted]	D2
[redacted]	D4
[redacted]	D6
[redacted]	
[redacted]	D8
[redacted]	DA

*Refer to specific iSBX product manual for details
**Odd I/O port address reserved for 16-bit operation on other products.

Table 1-1. Board Specifications (Continued)

INTERFACES	
Multibus	All signals TTL compatible
Parallel I/O	All signals TTL compatible
Interrupt Reqeusts	All signals TTL compatible
Interval Timer	All signals TTL compatible
iSBX Bus	All signals TTL compatible
Serial I/O	RS 232C compatible; configurable as a data set or data terminal.

ELECTRICAL REQUIREMENTS

Configuration	+5Vdc	+12Vdc*	-12Vdc*	+5 Batt**
Standard Board, no ROM/EPROM	3.8A	25mA	23mA	400mA
Maximum Operating Requirements (with all options)	11.2A	2A	2A	700mA

*+12Vdc & -12Vdc are required for RS232 application only.
**For battery backup option only.

PHYSICAL CHARACTERISTICS	
Width	12.00 in. (30.48 cm)
Length	6.75 in. (17.15 cm)
Thickness	0.50 in. (1.27 cm)
Weight	14 oz. (388 grams)
ENVIRONMENTAL CHARACTERISTICS	
Minimum Power Requirements	20 Watts
Maximum Power Requirements	115 Watts
Minimum Heat Dissipation	344 gcal/minute (1.4 Btu/minute)
Maximum Heat Dissipation	1640 gcal/minute (6.6 Btu/minute)
Operating Temperature Range	0°C — 55°C
Operating Humidity Range	90% max non-condensing

CHAPTER 2
PREPARATION FOR USE

2-1. INTRODUCTION

This chapter provides specific information enabling you to install the iSBC 88/25 Single Board Computer into your system, with minimal effort. The board's default or factory configuration for RAM addressing, ROM/PROM size, and other variables are described, followed by procedures for altering the default configuration. In this manner the board will accommodate a variety of applications. To completely familiarize yourself with the flexibility of the iSBC 88/25 board, we recommend reading Chapters 2 and 3 before installation and use.

2-2. UNPACKING AND INSPECTION

Inspect the shipping carton immediately upon receipt for evidence of mishandling during transit. If the shipping carton is severely damaged or water-stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is not present when the carton is opened and the contents are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment contact the Intel Product Service HOTLINE to obtain a return authorization number and further instructions (see Section 5-2). A purchase order will be required to complete the repair. A copy of the purchase order should be submitted to the carrier with your claim.

2-3. INSTALLATION CONSIDERATIONS

There are several general requirements which should be considered prior to board installation and use. These requirements are discussed in Sections 2-4 through 2-6.

2-4. MINIMAL OPERATING REQUIREMENTS

The iSBC 88/25 board factory default configuration is described in Chapter 1. In order to operate the board you may need additional equipment. For most applications this will typically be the following:

a. CPU software, residing in on-board ROM/PROM (Section 2-7).

b. I/O connectors and cables (Sections 2-28; 2-32; 2-33).

c. Additional on-board RAM, if more than 4 bytes are required (Section 2-10).

d. Line drivers or terminators for parallel I/O lines (Section 2-12).

Instructions for installing these items are provided in the sections listed above.

2-5. POWER REQUIREMENTS

Three voltages are required for operating the iSBC 88/25 board in most configurations: +5Vdc, +12Vdc, and -12 Vdc. All must be within ±5% of absolute. However, some configurations do not require all voltages. Power requirements for the various board configurations are listed in Table 1-1. The table includes power required by an optional iSBC Multimodule board which may be installed.

2-6. COOLING REQUIREMENTS

Operating temperature range for the iSBC 88/25 board is 0° to 55°C. If the board is installed into an Intel system chassis, adequate cooling is provided by the fans supplied. However, if the board is used in another chassis, ensure adequate cooling is provided by taking temperature readings inside the chassis at the site environment.

2-7. ROM/PROM INSTALLATION

Sockets U33, U34 and U64, U65 are reserved for optional ROM/PROM devices. A maximum of 64K bytes may be installed in these four sockets, using four 16K byte 28-pin devices. A summary of compatible device types, capacity, and addressing is provided in Table 2-1. Device types may not be mixed, however empty sockets are allowed (provided they are not addressed).

Before installing the devices on the board several jumper connections may be required to specify device size and power scheme. Table 2-3 specifies the board's factory default jumper configuration (set for 2716 devices) and summarizes the other possible ROM/PROM jumper connections.

CAUTION

Never install any device onto a board when power is applied. Damaged to the board, device and power supply could result.

CAUTION

The ROM/PROM sockets are 28-pin sockets which are used for both 24-pin and 28-pin devices. When inserting devices, ensure that pin 1 of the ROM/PROM device corresponds with pin 1 of the socket. Use the upper white dot for 28-pin devices and the lower white dot for 24-pin devices (Figure 2-1).

Table 2-1 provides address ranges when the optional iSBC 341 ROM/PROM Expansion Module is installed on the iSBC 88/25 board. This operation will double the existing ROM space. The addressed listed include ROM/PROM space already on the iSBC 88/25 board. Refer to Section 2-9 for iSBC 341 board installation information. Refer to Section 2-22 for PROM Wait State information. The board is configured at the factory for 2716 type devices, requiring 2 wait states.

Table 2-1. ROM/PROM Configurations

	iSBC 88/25				iSBC 341			
	U33	U64	U34	U65	U2*	U5*	U3*	U6*
2716's	FF800-FFFFF	FF000-FF7FF	FE800-FEFFF	FE000-FE7FF	FD800-FDFFF	FD000-FD7FF	FC800-FCFFF	FC000-FC7FF
2732's	FF000-FFFFF	FE000-FEFFF	FD000-FDFFF	FC000-FCFFF	FB000-FBFFF	FA000-FAFFF	F9000-F9FFF	F8000-F8FFF
2764's	FE000-FFFFF	FC000-FDFFF	FA000-FBFFF	F8000-F9FFF	F6000-F7FFF	F4000-F5FFF	F2000-F3FFF	F0000-F1FFF
27840's	FC000-FFFFF	F8000-FBFFF	F4000-F7FFF	F0000-F3FFF	EC000-EFFFF	E8000-EBFFF	E4000-E7FFF	E0000-E3FFF

Table 2-2. RAM Configurations

	iSBC 88/25		iSBC 302*					
	U67	U51	U3	U5	U2	U6	U1	U4
Nibble	Low	High	High	Low	High	Low	Low	High
Address	0000 - 00FFF		01000 - 01FFF		02000 - 02FFF		03000 - 03FFF	
*Install jumper 94-187.								

Table 2-3. ROM/PROM Jumper Configurations

	DEVICE TYPE & SIZE			
	2716* 2K x 8	2732 4K x 8	2764 8K x 8	27840 16K x 8
J6 Jumpers	1 - 14 2 - 13 3 - 12	1 - 14 5 - 12 6 - 9	1 - 14 6 - 9	1 - 14 5 - 9 7 - 8
Decode PROM Jumpers	None	90 - 91	92 - 93	90 - 91 92 - 93
*Factory default				

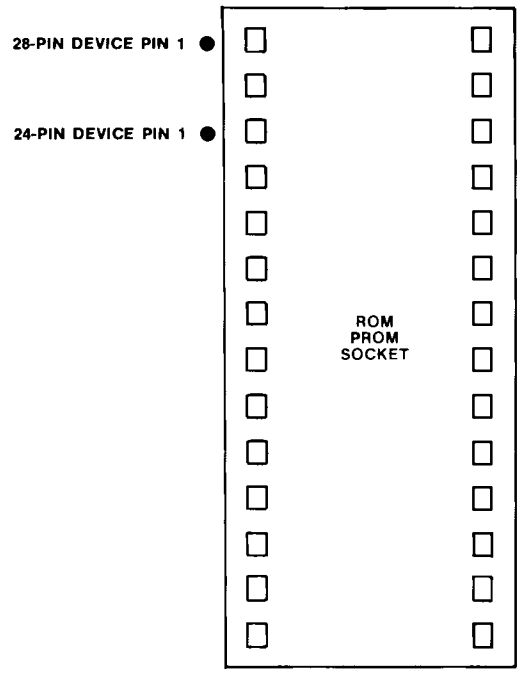


Figure 2-1. ROM/PROM Device Insertion

2-8. iSBC 341 MODULE INSTALLATION

The optional iSBC 341 ROM/PROM Expansion Module is designed to increase the amount of iSBC 88/25 on-board ROM/PROM. The size of the devices used on the module must match the size of the devices used on the board. For example, if the iSBC 88/25 board is equipped with 4K X 8 EPROM devices, the iSBC 341 module must also use 4K X 8 EPROM devices. The following procedure is recommended for iSBC 341 module installation:

a. Turn off power and remove iSBC 88/25 board from system.

b. Carefully remove ROM/PROM device from board socket U34 and install it into socket U1 on the iSBC 341 module. Similarly, remove the ROM/PROM device from board socket U65 and install it into socket U4 on the iSBC 341 module. Be sure to install these two devices in the sockets indicated.

c. Carefully insert all remaining ROM/PROM devices into the iSBC 341 module. Refer to CAUTION notice in Section 2-7 for related socket information.

d. Using the hardware supplied with the iSBC 341 module install it onto the iSBC 88/25 board. The module connector fits directly into ROM/PROM sockets U34 and U65 and board connector J7.

e. Install jumper connection 94-187 on the iSBC 88/25 board.

NOTE

When jumper 94-187 is installed both RAM *and* ROM / PROM memory areas are expanded.

f. Installation is complete. The iSBC 88/25 board is now ready to be installed into your system cardcage.

2-9. PAGE SELECT JUMPER CONFIGURATION

The iSBC 88/25 board is configured at the factory to recognize two separate on-board 128K byte pages as valid memory addresses. All on-board RAM must reside in an EVEN page, and all on-board ROM/PROM must reside in an ODD page. The default RAM page range is from address 0 - 1FFFF (hexadecimal) and the default ROM is from E0000-FFFFF. These pages may be altered by jumper selection as shown in Table 2-4.

Table 2-4. Page Select Jumpers

Function	Address Range	Jumper Connection
RAM ONLY	00000 - 1FFFF	96 - 95*
ROM/PROM ONLY	20000 - 3FFFF	99 - 95 or 103
RAM ONLY	40000 - 5FFFF	97 - 95 or 103
ROM/PROM ONLY	60000 - 7FFFF	101 - 95 or 103
RAM ONLY	80000 - 9FFFF	98 - 95 or 103
ROM/PROM ONLY	A0000 - BFFFF	102 - 95 or 103
RAM ONLY	C0000 - DFFFF	100 - 95 or 103
ROM/PROM ONLY	E0000 - FFFFF	104 - 103*

NOTE: * indicates factory default connections. Select any two pages; connect RAM page jumper post to post 95, ROM page to post 103.

2-10. ON BOARD RAM EXPANSION AND iSBC 302 RAM MODULE INSTALLATION

The iSBC 88/25 board is shipped with 4K bytes of static RAM in place. Two Intel 2168 RAM devices in sockets U51 and U67 are used in this configuration. An additional 8K bytes of expansion is provided by installing the optional iSBC 302 RAM Expansion Module providing a total of 12K bytes on board. Table 2-2 provides socket and addressing information for the iSBC 302 module. The following procedure is recommended for installing the RAM module.

a. Turn power off and remove the iSBC 88/25 board from its system.

b. Using the hardware supplied with the iSBC 302 module, install the module onto the iSBC 88/25 board. The iSBC 302 module connector pins fit directly into board sockets U52 and U68, and board connector J8. Ensure that all pins fit correctly before tightening the hardware.

c. Install jumper 94 - 187 on the iSBC 88/25 board.

NOTE

When jumper 94-187 is installed both RAM *and* ROM / PROM memory areas are expanded.

d. On-board RAM space with 12K bytes will cover 0-02FFF (hexadecimal).

e. iSBC 302 installation is complete. The iSBC 88/25 board is now ready to be installed into your system cardcage. See step (f) for 16K configuration.

f. Two additional 2168 RAM devices may be installed in iSBC 302 board sockets U1 and U4 to increase on-board RAM to 16K bytes. In this (maximum) configuration, on-board RAM addressing will cover 0-03FFF (hexadecimal).

NOTE

To avoid using two cardcage slots when the iSBC 302 module is installed, place the iSBC 88/25 board in slot J2 (top slot).

Table 2-5. iSBC 88/25™ Factory Default Jumper Summary

Schematic Sheet No.	Jumper Pair	Function	Schematic Sheet No.	Jumper Pair	Function
1	158-159	Battery Defeat	7	23-25	Gate 1 Control
			7	30-31	Gate 0 Control
2	1-2	Wait State Generator	7	53-54	PIT Input (1.23 MHz to CLK2)
2	4-6	Wait State Generator	7	~~55-56~~	~~PIT Input (1.23 MHz to CLK0)~~
2	9-10	Wait State Generator	7	57-58	PIT Input (153.6 KHz to CLK1)
2	13-14	Failsafe Timer	7	76-77	RxC Input
2	17-18	PROM BUSY	7	80-81	TxC Input
2	151-152	U45 CLK Output	7	86-87	U16 OSC Output
2	165-166	TEST ONLY	7	88-89	DSR/ Input
4	154-155	U44 ALE Output	8	26-27	Parallel Port A Direction
4	156-157	U44 DT/R Output	8	35-39	Parallel Port C Bit 5
4	160-161	ANYRQST (See Sect. 2-24)	8	36-40	Parallel Port C Bit 6
4	163-164	BCLK/ To Multibus	8	37-41	Parallel Port C Bit 7
4	168-169	CBRQ/ To Ground	8	38-42	Parallel Port C Bit 4
4	170-171	BPRO/ To Multibus	8	43-47	Parallel Port C Bit 0
4	183-184	CCLK/ To Multibus	8	44-48	Parallel Port C Bit 1
			8	45-49	Parallel Port C Bit 2
5	~~95-99~~	~~RAM Page Addr: 00000-1FFFF~~	8	46-50	Parallel Port C Bit 3
5	~~103-104~~	~~PROM Page Addr: E0000-FFFFF~~			
			9	~~109-110~~	~~NMI Gate~~
6	~~143-145~~	~~RAM Size (4K Bytes)~~	9	~~113-115~~	~~Interrupt IR2~~
6	J6, 1-14	PROM Size (2716)	9	~~114-121~~	~~Interrupt IR0~~
6	J6, 2-13	PROM Size (2716)	9	~~120-124~~	~~Interrupt IR5~~
6	J6, 3-12	PROM Size (2716)	9	149-150	ON BD ADR/

Table 2-5A. iSBC 88/25 Numerical Jumper List

Schematic Sheet No.	Jumper Pair	Function	Schematic Sheet No.	Jumper Pair	Function
2	1-2*	1 I/O Wait State	5	92-93	PROM Size (2764)
2	2-3	2 I/O Wait States	5	94-187	RAM Size > 4K Bytes
2	4-6*	1 PROM Wait State	5	95-100	RAM Page Addr. C0000-DFFFF
2	5-6	0 PROM Wait State	5	95-96*	RAM Page Addr. 00000-1FFFF
2	6-7	2 PROM Wait States	5	95-97	RAM Page Addr. 40000-5FFFF
2	6-8	3 PROM Wait States	5	95-98	RAM Page Addr. 90000-9FFFF
2	9-10*	2 INT ACK Wait States	5	99-103	PROM Page Addr. 20000-3FFFF
2	10-11	3 INT ACK Wait States	5	101-103	PROM Page Addr. 60000-7FFFF
2	13-14*	Failsafe Timer	5	102-103	PROM Page Addr. A0000-BFFFF
9	15-16	+5Vdc Output To J1-50	5	103-104*	PROM Page Addr. E0000-FFFFF
2	17-18*	PROM BUSY	9	106-Matrix	iSBX 2 INT0
8	20-CC Bit	Secondary TxD Channel	9	107-Matrix	Power Fail INT (PFIN/)
8	21-CC Bit+	EXT CLK/	9	108-Matrix	External INT (EXT INTR0)
8	22-CC Bit	OVERRIDE/ Multibus	9	109-110*	NMI Gate
7	23-25*	Gate 1 Control	9	111-Matrix	TIMER1 INTR
8	23-CC Bit	PIT Gate 1 Control	9	112-113*	Interrupt IR2
8	24-CC Bit	NMI Input Gate	9	112-Matrix	TIMER0 INTR
8	26-27*	Parallel Port A Direction	9	114-121*	Interrupt IR0
8	26-CC Bit	Programmable C8 Direction	9	114-Matrix	SIRxINTR
8	28-CC Bit+	PB INTR	9	115-Matrix	iSBX 2 INT1
8	29-CC Bit+	BUS INTR OUT to Multibus	9	118-Matrix	EDGE INTR
7	30-31*	Gate 0 Control	9	123-Matrix	SITxINTR
8	31-CC Bit	PIT Gate 0 Control	9	124-Matrix	P1-42 Multibus INT1/
8	32-CC Bit+	PA INTR	9	125-Matrix	iSBX 1 INT0
8	33-CC Bit	TEST/ Input	9	126-Matrix	iSBX 1 INT1
8	34-CC Bit+	PFSN/ Power Fail Sense Input	9	127-Matrix	8087 Math INT (MINT)
8	[illegible]	Parallel Port C Bit 5	9	128-Matrix	PB INTR
8	[illegible]	Parallel Port C Bit 6	9	129-Matrix	PA INTR
8	[illegible]	Parallel Port C Bit 7	9	130-Matrix	P1-39 Multibus INT2/
8	[illegible]	Parallel Port C Bit 4	9	131-Matrix	P1-40 Multibus INT3/
8	[illegible]	Parallel Port C Bit 0	9	132-Matrix	P1-41 Multibus INT0/
8	[illegible]	Parallel Port C Bit 1	9	133-134*	Interrupt IR5
8	[illegible]	Parallel Port C Bit 2	9	134-Matrix	P1-38 Multibus INT5/
8	[illegible]	Parallel Port C Bit 3	9	135-Matrix	P1-37 Multibus INT4/
8	[illegible]	[illegible]	9	136-Matrix	P1-36 Multibus INT7/
7	53-54*	PIT Input (1.23 MHz to CLK2)	9	137-Matrix	P1-35 Multibus INT6/
7	53-59	External CLK to CLK2 Input	9	138-Matrix	Power Line Clock (PLC)
7	53-61	2.46 MHz to CLK2 Input	6	[illegible]	[illegible]
7	53-62	Output 1 to CLK2 Input	9	149-150*	ON BD ADR/
7	53-63	PLC to CLK2 Input	2	151-152*	U45 CLK Output
7	53-56*	PIT Input (1.23 MHz to CLK0)	4	154-155*	U44 ALE Output
7	55-58	1.23 MHz to CLK1 Input	4	156-157*	U44 DT/R Output
7	56-59	External CLK to CLK0 Input	1	158-159*	Battery Defeat
7	56-60	Output 0 to CLK1 Input	4	160-161*	Bus Arbiter (See Sect. 2-24)
7	56-61	2.46 MHz to CLK0 Input	4	160-161+	Bus Arbiter Config. #2
7	56-63	PLC to CLK0 Input	4	161-162+	Bus Arbiter Config. #1
7	57-58*	PIT Input (153.6 KHz to CLK1)	4	163-164*	CLK/ To Multibus
7	58-59	External CLK to CLK1 Input	2	165-166*	TEST ONLY
7	58-61	2.46 MHz to CLK1 Input	4	167-168+	Bus Arbiter Config. #1
7	58-63	PLC to CLK1 Input	4	167-168+	Bus Arbiter Config. #2
1	65-66	+5Vdc to J2-23	4	168-169*+	Bus Arbiter (See Sect. 2-24)
1	67-68	-12Vdc to J2-19	4	170-171*	BPRO/ To Multibus
7	69-70	Secondary TxD Input	9	172-173	INT4/ Output To P1-37
7	69-71	Secondary TxC Input	9	172-174	INT2/ Output To P1-39
7	72-73	STxD/STxC to J2-26	9	172-175	INT5/ Output To P1-38
7	73-74	STxD/STxC to J2-21	9	172-176	INT3/ Output To P1-40
7	73-75	STxD/STxC to J2-5	9	172-177	INT7/ Output To P1-36
7	[illegible]-77*	RxC Input	9	172-178	INT0/ Output To P1-41
7	76-78	External RxC Input	9	172-179	INT6/ Output To P1-35
7	79-80	External TxC Input	9	172-180	INT1/ Output To P1-42
7	80-81*	TxC Input	4	183-184*	CCLK/ To Multibus
1	82-83	+12Vdc to J2-22	6	J6, 1-14*+	PROM Size (2716)
7	84-85	RTS/ to CTS/	5	J6, 1-14*+	PROM Size (2732)
7	86-87*	U16 OSC Output	6	J6, 2-13*+	PROM Size (2716)
7	88-89*	DSR/ Input	6	J6, 3-12*+	PROM Size (2716)
5	90-91	PROM Size (2732)	5	J6, 3-12*+	PROM Size (2732)
5	90-91+92-93	PROM Size (27840)	5	J6, 6-9+	PROM Size (2732)

* = Factory default installation.
\+ = Requires additional jumper installation; see text.

2-11. BYTE-WIDE RAMS

The iSBC 88/25 board will accept the so called "byte wide" RAMs. These 28-pin RAM devices such as the Intel 2188, 8K x 8 dynamic RAMs, are inserted into ROM / PROM sockets U34 and/or U65 (lower two locations of ROM space). Any byte wide RAMs used on the iSBC 88/25 board must be of the same size (capacity) as the ROM residing in socket U33 (top location). For example if the ROM in U33 is a 2K x 8 device, the byte wide RAM in location U65 must also be 2K x 8. Byte wide RAMs may also reside on the iSBC 341 ROM Expansion Module (all sockets). Devices on the iSBC 341 module must also be the same size as the ROM in socket U33.

The following jumper modifications are required when using 28-pin byte wide RAMs in ROM sockets:

a. Install jumper 141 - 142.

b. Verify J6 strapping with Table 2-3. Byte wide RAMs installed must be of the same size as uppermost ROM (in socket U33). Table 2-3 correlates device size to proper J6 strapping.

2-12. LINE DRIVERS AND I/O TERMINATORS

When using parallel ports CA and CC, line drivers or terminators are required for operation. The iSBC 88/25 board is equipped with a bidirectional bus transceiver on parallel port C8. Sockets U8 through U11 are provided for line driver/terminator devices. Table 2-6 lists the types of terminators and line drivers which are recommended for this purpose.

2-13. JUMPER CONFIGURATIONS

Much of the flexibility of your iSBC 88/25 board is due to the use of jumper connections which may easily be altered from their factory configurations to suit your particular application. Selections 2-14 through 2-35 describe optional jumper connections for all of the iSBC 88/25 configurations. Table 2-5 lists the factory default jumper connections on the board. Table 2-5A lists most board jumpers. Physical location of jumper posts on the board are shown in Figure 5-1. Jumper connections are also shown schematically in Figure 5-2.

2-14. INTERVAL TIMER JUMPER CONFIGURATIONS

The 8253-5 Programmable Interval Timer (PIT) is configured at the factory with three jumpers installed, as shown in Table 2-7. These three jumpers select the input frequencies to each of the three independent counters within the PIT. Outputs 0 and 1 from the timer are routed directly to the interrupt matrix (Section 2-18). These outputs may then be jumpered to the desired on-board interrupt level, or routed off-board via the Multibus interrupt lines, by connection to one of the outboard posts (173 through 180).

Output 2 is used for the 8251A Programmable Communications Interface (PCI) transmit and receive clocks.

Table 2-6. Line Driver and Terminator Circuits

Line Drivers	Current	I/O Terminators
7400 I	16 mA	iSBC 901
7403 I, OC	16 mA	
7408 NI	16 mA	iSBC 902
7409 NI, OC	16 mA	

I = inverting; NI = non-inverting; OC = open collector.

2-15. SERIAL PORT JUMPER CONNECTIONS

The iSBC 88/25 board serial port is configured at the factory to the RS 232C standard interface. The board

Table 2-7. Interval Timer Input Jumper Configurations

Function	Jumpers	Description
2.46 MHz	56 - 61	Optional input to CLK 0
	58 - 61	Optional input to CLK 1
	53 - 61	Optional input to CLK 2
1.23 MHz	55 - 56*	Default input to CLK 0
	53 - 54*	Default input to CLK 2
	55 - 58	Optional input to CLK 1
153.6 KHz	57 - 58*	Default input to CLK 1
Output 0	60 - 56	Optional cascade mode (Output 0 to CLK 1)
Output 1	62 - 53	Optional cascade mode (Output 1 to CLK 2)
Output 2	61 - xx	Optional cascade mode (Output 2 to xx)
External Clock	59 - xx	Connect to 53, 56, 58 for external input
Power Line Clock	63 - xx	Connect to 53, 56, 58 for 2x line frequency if using iSBC 665 Modular Chassis

NOTE: * indicates default connection; select one function per input only. xx indicates Variable Choice.

assumes the data set role. The serial port uses I/O connector J2. Jumper connections associated with the serial port are summarized in Table 2-8. Connector J2 pin assignments are provided in Table 2-9.

Table 2-8. Serial Port Jumper Configurations

Function	Jumpers	Description
[illegible]	[illegible]*	[illegible]
[illegible]	[illegible]*	[illegible]
External TxC	79 - 80	Connects J2-7 to TxC
External RxC	76 - 78	Connects J2-7 to RxC
Secondary TxC	79 - 71	Use with on board or external TxC clock
Secondary TxD	79 - 70	Use with parallel port CC bit and STxC
	72 - 73	Connects STxD/STxC to J2-26
	73 - 75	Connects STxD/STxC to J2-5
	73 - 74	Connects STxD/STxC to J2-21
RTS/ to CTS/	84 - 85	Straps on board RTS/ to CTS/
Voltages	65 - 66	Connects +5 Vdc to J2-23
	82 - 83	Connects +12 Vdc to J2-22
	67 - 68	Connects -12 Vdc to J2-19
DSR Defeat	88 - 89*	Disconnects DSR input when removed

NOTE: * indicates default connection installed.

Table 2-9. Connector J2 Pin Assignments

Pin No.[1]	iSBC 88/25 Signal	RS-232C Pin No.[2]	PCI Function
J2 - 1	Not Used	14	—
J2 - 2	Ground	1	GND
J2 - 3	Not Used	15	—
J2 - 4	Transmitted Data	2	RxD Input
J2 - 5	See J2 - 26[3]	16	See J2 - 26
J2 - 6	Received Data	3	TxD Output
J2 - 7	External Clock	17	TxC/RxC Input
J2 - 8	Request To Send	4	CTS/ Input
J2 - 9	Not Used	18	—
J2 - 10	Clear To Send	5	RTS/ Output
J2 - 11	Not Used	19	—
J2 - 12	Data Set Ready	6	DSR/ Input
J2 - 13	Data Terminal Ready	20	DTR/ Output
J2 - 14	Ground	7	GND
J2 - 15	Not Used	21	—
J2 - 16	Not Used	8	—
J2 - 17	Not Used	22	—
J2 - 18	Not Used	9	—
J2 - 19	-12 Vdc[3]	23	—
J2 - 20	Not Used	10	—
J2 - 21	See J2 - 26[3]	24	See J2 - 26
J2 - 22	+12 Vdc[3]	11	—
J2 - 23	+5 Vdc[3]	25	—
J2 - 24	Not Used	12	—
J2 - 25	Ground	—	GND
J2 - 26	Secondary TxD or Clock Out[3]	13	STxD or TxC/TxD

NOTES:
1. Odd numbered pins are on component side of board; even pins on solder side.
2. Cable connector numbering convention may not correspond with J2 numbering.
3. Not connected at factory.

2-16. PARALLEL PORT JUMPER CONFIGURATIONS

Parallel port CC has a jumper matrix between the 8255A-5 PPI device and the driver/terminator sockets U8 and U9. This arrangement allows a greater amount of flexibility when using these lines. Parallel port C8 has an 8287 inverting Bus Transceiver installed in socket U7. (An 8286 non-inverting device could be used, if desired.) The transceiver control line is configured at the factory for the output mode. Refer to Section 2-17 for instructions on converting this mode. Parallel port CA operation is determined entirely by software programming and the type of devices installed in sockets U10 and U11.

Refer to Table 2-10 for a list of operating modes which are allowed for each parallel port.

Table 2-10 provides the default connections for all parallel ports, and shows the corresponding input/output connector pin numbers. Table 2-11 provides jumper information and descriptions of the optional features associated with the port CC jumper matrix. Table 2-12 is a comprehensive guide to mode restrictions and jumper connections for all three parallel ports.

Before configuring the parallel ports for your application, refer to Section 3-22 for 8255A-5 programming information.

Table 2-10. Parallel Port Default Jumper Connections

Port CC Bit	Mode/Direction	Jumper Conn.	J1 Pin Number
0	0 Input	43 - 47	J1 - 24
1	0 Input	44 - 48	J1 - 22
2	0 Input	45 - 49	J1 - 20
3	0 Input	46 - 50	J1 - 18
4	0 Input	38 - 42	J1 - 26
5	0 Input	35 - 39	J1 - 28
6	0 Input	36 - 40	J1 - 30
7	0 Input	37 - 41	J1 - 32

NOTE: Driver/Terminators not installed at factory.

Port C8 Bit	Mode/Direction	Jumper Conn.	J1 Pin Number
0	0 Output	NONE	J1 - 48
1	0 Output		J1 - 46
2	0 Output		J1 - 44
3	0 Output		J1 - 42
4	0 Output		J1 - 40
5	0 Output		J1 - 38
6	0 Output		J1 - 36
7	0 Output		J1 - 34

NOTE: For other modes see Section 2-14.

Port CA Bit	Mode/Direction	Jumper Conn.	J1 Pin Number
0	0 Output	NONE	J1 - 16
1	0 Output		J1 - 14
2	0 Output		J1 - 12
3	0 Output		J1 - 10
4	0 Output		J1 - 8
5	0 Output		J1 - 6
6	0 Output		J1 - 4
7	0 Output		J1 - 2

NOTE: Driver/Terminators not installed at factory.

2-17. PORT C8 TRANSCEIVER CONVERSION

Port C8 is equipped with an 8287 inverting Bus Transceiver installed in socket U7. The transceiver is default connected to operate in the output only mode, with jumper 26-27. Two other modes are possible for the transceiver:

a. *Input only mode:* remove 26-27 and install 26-30.

b. *Programmable mode:* remove 26-27 or 26-30 and install a jumper between post 26 and the bit you select from port CC to control the port direction. (Connect to post on device side of port CC matrix.) The transceiver's direction or mode is then controlled by outputting the appropriate bit state to the device.

0 = output only mode
1 = input only mode

2-18. INTERRUPT MATRIX JUMPER CONFIGURATIONS

The iSBC 88/25 board provides jumper posts for 12 on-board interrupt sources and 11 off-board sources. Any eight of these sources can be interfaced to the 8259A Programmable Interrupt Controller (PIC) through the on-board interrupt matrix. The PIC provides eight interrupt levels. In addition the 8088 CPU can utilize its NMI input for high priority interrupt requests.

In the factory default configuration, the following four interrupt matrix jumpers are installed:

a. 112-113 Timer 0 output to IR2 on PIC

b. 133-134 Multibus interrupt INT5/ to IR5 on PIC

c. 109-110 Disable NMI Mask gate

d. 114-121 RxRDY Interrupt

Table 2-11. Parallel Port CC Jumper Configurations

Function	Jumpers	Description
OUTPUTS:		
EXT CLK/	21 - xx	Connect to desired jumper post on connector side of parallel matrix; driver terminator socket must have terminator. See Table 2-5 for required timer jumper installation.
OVERRIDE/	22 - xx	Software programmable Multibus override control. Connects to desired bit on device side of parallel matrix.
SECONDARY TxD	20 - xx	Software programmable transmit channel. Connects to desired bit on device side of parallel matrix.
PA INTR	32 - xx	Parallel port interrupt "A". Software programmable on board interrupt. Connects to desired bit on device side of parallel matrix. See Table 2-11 for associated required jumper connection.
PB INTR	28 - xx	Parallel port interrupt "B". Software programmable on board interrupt. Connect to desired bit on device side of parallel matrix. See Table 2-11 for associated required jumper connection.
TEST/	33 - xx	Software programmable TEST/ input. When not asserted, causes the 8088 to either execute WAIT states or become idle until asserted.
BUS INTR OUT	29 - xx	Software programmable Multibus (System) interrupt output. Requires additional connection from jumper post 172 to desired output post (173 through 180). See Schematic sheet 9 for levels.
GATE 0 CNTRL	31 - xx	Software programmable gate input for 8253A PIT. Connect to desired bit on device side of parallel matrix.
GATE 1 CNTRL	23 - xx	Software programmable gate input for 8253A PIT. Connect to desired bit on device side of parallel matrix.
NMI MASK/	24 - xx	Software programmable means to switch the 8088 NMI input on or off. A low disables the NMI input gate. Connect to desired bit on device side of parallel matrix.
DS1	51 - 52	Software programmable indicator lamp. Lamp is connected to bit 3 of port CC. Install jumper to enable.
PORT C8 DIRECTION	26 - xx	Controls direction (input or output) of port C8. Refer to Section 2-17.
INPUT:		
PFSN/	34 - xx	Power fail sense line. This line is an output from an off-board latch which indicates a power failure has occurred. PFSN/ may be read by the parallel port. In conjunction with a battery backup power-on sequence. Refer to Section 2-34. Connect post 34 to one of the available input lines.

NOTE: xx denotes variable bit choice. Only one function per bit is allowed.

Table 2-13 provides a complete list of possible interrupt jumper configurations on the iSBC 88/25 board. Refer to Section 3-27 for 8259A programming information.

Table 2-12. Parallel Port Jumpers and Restrictions

Port	Mode	Driver (D)/ Terminator (T)	Jumper Configuration			Restrictions	
			Delete	Add	Effect	Port	
C8	0 Input	8287: U7	26-27*	26-30	8287 = input enabled.	CA	None, can be mode 0 or 1, input or output.
						CC	None, can be in mode 0, input or output, unless Port CA is in Mode 1.
C8	0 Output (latched)	8287: U7		26-27*	8287 = output enabled.	CA	None, can be in Mode 0 or 1 input or output.
						CC	None can be in Mode 0, input or output, unless Port CA is in Mode 1.
C8	1 Input (strobed)	8287: U7 T: U8 D: U9	26-27*	26-30	8287 = input enabled.	CA	None, can be in mode 0 or 1 input or output.
			35-39*	38-42*	Connects J1-26 to STB_A/ input.	CC	Port CC bits perform the following:
			35-39* and 46-50*	39-46	Connects IBF_A output to J1-18.		• Bits 0, 1, 2 - Control for Port CA if Port CA is in Mode 1.
				32-50	Connects INT_A output to PAINTR		• Bit 3 - Port C8 interrupt jumper matrix.
							• Bit 4 - Port C8 Strobe (STB/) input.
							• Bit 5 - Port C8 Input Buffer Full (IBF) output.
							• Bits 6, 7 - Port CC input or output (both, must be in same direction).
C8	1 Output (latched)	8287: U7 T: U8 D: U9		26-27*	8287 = output enabled.	CA	None; can be in Mode 0 or 1, input or output.
				36-40*	Connects J1-30 to ACK_A/ input.	CC	Port EA bits perform the following:
			46-50* and	41-46	Connects OBF_A output to J1-18.		• Bits 0, 1, 2 - Control for Port CA if Port CA is in Mode 1.
				32-50	Connects INT_A output to interrupt matrix.		• Bit 3 - Port C8 interrupt (PA INTR) to interrupt jumper matrix.
							• Bits 4, 5 - Port CC input or output (both must be in same direction).
							• Bit 6 - Port C8 Acknowledge (ACK/) input.
							• Bit 7 - Port C8 Output Buffer Full (OBF/) output.

*Default jumper connected at the factory.

Table 2-12. Parallel Port Jumpers and Restrictions (Continued)

Port	Mode	Driver (D)/ Terminator (T)	Jumper Configuration			Restrictions	
			Delete	Add	Effect	Port	
C8	2 (bidirectional)	8287: U7 T: U8 D: U9	26-27*	26-36	Allows ACK_A/ input to control 8287 in/out	CA	None; can be in Mode 0 or 1, intput or output.
						CC	Port CC bits perform the following:
				38-42*	Connects J1-26 to STB_A/ input.		• Bit 0 - Can only be used for jumper option.
			35-39* and 43-47*	39-43	Connects IBF_A output to J1-24.		• Bits 1, 2 - Can be used for input or output if Port CA is in Mode 0.
				36-40*	Connects J1-30 to ACK_A/ input.		• Bit 3 - Port C8 interrupt (PA INTR) to interrupt jumper matrix.
			37-41* and 46-50	41-46	Connects OBF_A/ output to J1-18.		• Bit 4 - Port C8 Strobe (STB/) input.
				32-50	Connects INT_A output to interrupt matrix.		• Bit 5 - Port C8 Input Buffer Full (IBF) output.
							• Bit 6 - Port C8 Acknowledge (ACK/) input.
							• Bit 7 - Port C8 Output Buffer Full (OBF/) output.
CA	0 Input	T: U10, U11	None	None		C8	None.
						CC	None; Port CC can be in Mode 0, input or output, if Port C8 is also in Mode 0.
CA	0 Output (latched)	D: U10, U11	None	None		C8	None
						CC	None; Port CC can be in Mode 0, input or output, if Port C8 is also in Mode 0.
CA	1 Input (strobed)	T: U8, U10, U11 D: U9		44-48*	Connects IBF_B output to J1-22.	C8	None.
						CC	Port CC bits perform the following:
			37-41* and 45-49*	37-49	Connects J1-32 to STB_B/ input.		• Bit 0 - Port CA interrupt (PB INTR) to interrupt jumper matrix.
				28-47	Connects INT_B output interrupt matrix.		• Bit 1 - Port CA Input Buffer Full (IBF) output.
							• Bit 2 - Port CA Strobe (STB/) input.
							• Bit 3 - If Port C8 is in Mode 0, bit 3 can be input or output. Otherwise, bit 3 is reserved.
							• Bits 4, 5, 6, 7 - Depends on Port C8 mode.

*Default jumper connected at the factory.

Table 2-12. Parallel Port Jumpers and Restrictions (Continued)

Port	Mode	Driver (D)/ Terminator (T)	Jumper Configuration			Restrictions	
			Delete	Add	Effect	Port	
CA	1 Output (latched)	T: U8 D: U9, 10, 11		44-48*	Connects OBF_B/ outpt to J1-22.	C8	None.
						CC	Port CC bits perform the following: • Bit 0 - Port CA interrupt (PB INTR) to interrupt jumper matrix. • Bit 1 - Port CA Output Buffer Full (OBF/) output. • Bit 2 - Port CA Acknowledge (ACK/) input. • Bit 3 - If Port C8 is in Mode 0, bit 3 can be input or output. Otherwise, bit 3 is reserved. • Bits 4, 5, 6, 7 - Depends on Port C8 mode.
			37-41* and 45-49*	37-49	Connects J1-32 to ACK_B/ input.		
			43-47*	28-47	Connects INT_B output to interrupt matrix.		
CC (upper)	0 Input	T: U8	None	38-42* 35-37* 36-40* 39-41*	Connects bit 4 to J1-26 Connects bit 5 to J1-28 Connects bit 6 to J1-30 Connects bit 7 to J1-32	C8	Port C8 must be in Mode 0 for all four bits to be available.
						CA	Port CA must be in Mode 0 for all four bits to be available.
CC (lower)	0 Input	T: U9	None	43-47* 44-48* 45-49* 46-50*	Connects bit 0 to J1-24 Connects bit 1 to J1-22 Connects bit 2 to J1-20 Connects bit 3 to J1-18	C8	Port C8 must be in Mode 0 for all four bits to be available.
						CA	Port CA must be in Mode 0 for all four bits to be available.
CC (upper)	0 Output (latched)	D: U8	None	Same as for Port CC (upper) Mode 0 input.		C8	Same as for Port CC (upper) Mode 0 input.
CC (lower)	0 Output (latched)	D: U9	None	Same as for Port CC (lower) Mode 0 input.		CA	Same as for Port CC (lower) Mode 0 input.

*Default jumper connected at the factory.

In addition, the iSBC 88/25 board will support Multibus vectored interrupts from off-board slave 8259A interrupt controllers. Refer to Section 2-19 for information on Multibus vectored interrupts.

The following sections provide brief descriptions of all interrupt request lines which are part of the interrupt matrix or related to the iSBC 88/25 board interrupt structure.

iSBX Multimodule Interrupt (SBX1 INT0,1; SBX2 INT0,1)

Two interrupt request lines are available for each iSBC Multimodule board installed on the iSBC 88/25 board.

Interval Timer Outputs (TIMER0,1 INTR)

These two lines come directly from 8253-5 Interval Timer. The timer 0 line is jumpered at the factory to interrupt request line IR2 (112-113). The timer 1 output is not connected at the factory.

Parallel Port Interrupts A, B (PA INTR & PB INTR)

Essentially these two lines are software programmable interrupt lines. Connect each line to the desired interrupt request input. Refer to Sections 2-13 for instructions on installing the parallel port matrix jumpers required for this option.

Transmit and Receive Interrupts (SITxINTR & SIRxINTR)

These signals originate at the 8251A Programmable Communications Interface (PCI) device. The signal SITxINTR is equivalent to TxRDY on the PCI and when true indicates that the PCI is ready to accept a data character from the CPU. Likewise, SIRxINTR is equivalent to RxRDY and when true indicates that the PCI contains a data character to be read by the CPU. Refer to the Intel Component Data Catalog for additional PCI information.

Power Line Clock (PLC)

This external signal is supplied by the iSBC 665/666 Modular Chassis, or similar circuit. It enters the board via auxiliary connector pin P2-31 and is specified at 120 Hz (double the AC line frequency).

Math Interrupt (MINT)

This signal originates from the optional iSBC 337 Numeric Data Processor Multimodule board. This interrupt is used only in conjunction with this option. Refer to Appendix C for additional iSBC 337 information.

Power Fail Interrupt (PFIN/)

Furnished by the iSBC Power Supply (or equivalent), this signal indicates that an AC lines power failure has occurred and DC voltage loss is imminent. Typically, this signal is jumpered to the NMI input on the 8088 CPU and is used in conjunction with a user written power down routine and battery backup scheme. Refer to Section 2-32 for additional battery backup information.

External Interrupt (EXT INTR)

This external interrupt signal enters the board via parallel port connector P2-50. The incoming signal is inverted by the iSBC 88/25 board, therefore a low state will activate the interrupt request (level mode), or a high to low transition (edge sensitive mode).

Single Request Edge Sensitive Feature (EDGE INTR)

The iSBC 88/25 board is equipped with special circuitry which allows you to operate a single interrupt request line in the edge sensitive mode, while the 8259A Interrupt Controller is in the level or edge mode. This feature is extremely useful when a critical request typically expires before the controller can acknowledge or service the request.

To enable EDGE INTR three jumper connections are required: first install a jumper from the desired interrupt source to jumper post 12 (post 12 is the EDGE latch input). Then install a jumper between post 118 and the desired interrupt request input on the 8259A controller (post 118 is the EDGE latch output). Install the third jumper to post 105, from the desired parallel port output bit (post 105 is the Clear input to the EDGE latch). Clearing the EDGE latch requires the parallel port to output a low (zero) to the latch. The latch should be cleared after the interrupt is serviced.

~~Example: a typical example configuration using the EDGE INTR is implemented using the on-board failsafe timer (Section 2-20) as the interrupt source for the EDGE latch. This requires a jumper from post 13 to post 12 (post 13 is the acknowledge timeout output). The second jumper is then installed between post 118 and post 122. This jumper connects the output of the latch to IR1 on the interrupt controller. The third jumper is installed from post 49 to post 105. This jumper connects parallel port bit 2 to the Clear input of the EDGE latch. The parallel port bit is then used to clear the latch after the interrupt is serviced, by writing a zero to that particular bit (see Section 2-14). Any port CC bit could be used to clear the latch.~~

Non-Maskable Interrupt Input Mask

The 8088 CPU NMI input may be configured to be software selectable. This is called the Non-Maskable Interrupt Input Mask on the iSBC 88/25 board. Two jumper connections are required to enable this option: first, remove jumper connection 109-110 and install a jumper between interrupt matrix post 109 and the desired interrupt source (i.e., PFIN/). Then install another jumper between post 24 and the desired parallel port CC bit post. A high state on this line will enable the mask gate. A low state will disable the mask gate, preventing any non-maskable interrupts from reaching the 8088 CPU.

Multibus Interrupt Output Option (BUS INTR OUT)

The iSBC 88/25 board has an optional parallel port configuration which provides a software programmable interrupt output. This would allow you to issue an interrupt request on a system Multibus line with one of the parallel ports CC bits. Two connections are required for this scheme: one jumper connection from the desired port CC bit to jumper post 29 and another jumper connection from jumper post 172 and the desired Multibus Interrupt Line. Refer to Tables 2-13 and 2-14.

Table 2-13. Interrupt Matrix Jumper Configurations

MATRIX INPUTS	DESCRIPTION	JUMPER POSTS IN	JUMPER POSTS OUT	MATRIX OUTPUTS
iSBX 2 INT0	J4 Multimodule INT 0	106	121	IR0 Input
iSBX 2 INT1	J4 Multimodule INT 1	115		
iSBX 1 INT0	J3 Multimodule INT 0	125		
iSBX 1 INT1	J3 Multimodule INT 1	126		
TIMER0 INTR	PIT Output 0	112	122	IR1 Input
TIMER1 INTR	PIT Output 1	111		
PA INTR	Parallel Port INT A	129	113	IR2 Input
PB INTR	Parallel Port INT B	128		
SITxINTR	PCI Transmit INT	123	120	IR3 Input
SIRxINTR	PCI Receive INT	114		
PLC	Power Line Clock	133	119	IR4 Input
MINT	8087 Math Chip INT	127		
PFIN/	Power Fail INT	107		
EXT INTR0	External INT from J1-50	108		
EDGE INTR	Edge Sensitive Mode INT			
INT0/	Multibus INT from P1-41	132	133	IR5 Input
INT1/	Multibus INT from P1-42	124		
INT2/	Multibus INT from P1-39	130		
INT3/	Multibus INT from P1-40	131	117	IR6 Input
INT4/	Multibus INT from P1-37	135		
INT5/	Multibus INT from P1-38	134	116	IR7 Input
INT6/	Multibus INT from P1-35	137		
INT7/	Multibus INT from P1-36	136		
GND	Ground	110	109	NMI Gate

NOTE:
Connect the desired IN jumper post to the desired OUT post. The following jumpers are factory installed: 112 - 113; 133 - 134; 109 - 110; and 114 - 121.

Table 2-14. Multibus™ Interrupt Output Jumper Configurations

OUTPUT LINE	P1 PIN	JUMPER POST	BUS INTR OUT POST
INT0/	P1-41	178	
INT1/	P1-42	180	
INT2/	P1-39	174	
INT3/	P1-40	176	172
INT4/	P1-37	173	
INT5/	P1-38	175	
INT6/	P1-35	174	
INT7/	P1-36	177	

NOTE:
Connect one jumper only from desired Multibus jumper post to the Bus Interrupt Output post (172). This option also requires a parallel port jumper matrix connection — see Section 2-15.

2-19. MULTIBUS VECTORED INTERRUPTS

The iSBC 88/25 board has the capability to service interrupt request which originate with a request to a slave, off-board 8259A Programmable Interrupt Controller (PIC). The slave INTR output is connected to the master PIC on the iSBC 88/25 board via the Multibus lines, as shown in Figure 2-2. This type of interrupt request is called a Bus Vectored Interrupt.

In general, a bus vectored interrupt should be of lower priority than interrupt requests which are input directly to the master PIC. The iSBC 88/25 board is not configured at the factory to accept bus vectored interrupts. To enable this feature, you must remove jumper 149-150.

Figure 2-2 shows, as an example, the on-board PIC (master) interfaced with two slave PIC devices. This arrangement leaves the master PIC with six inputs (IR2 through IR7) that can be used to handle the various on-board interrupt functions. The example scheme is implemented by programming the master PIC to handle IR0 and IR1 as bus vectored interrupts.

Each interrupt input (IR0 through IR7) to the master PIC may be individually programmed to be bus vectored or non-bus vectored. In the bus vectored mode, the slave PIC generates the interrupt type and in the non-bus vectored mode the master PIC generates the interrupt type.

Slave PIC devices must be identified as such during their initialization sequences (with ICW3). The master PIC must also be initialized to support slave PIC devices. Section 3-27 describes 8259A programming and provides initialization examples.

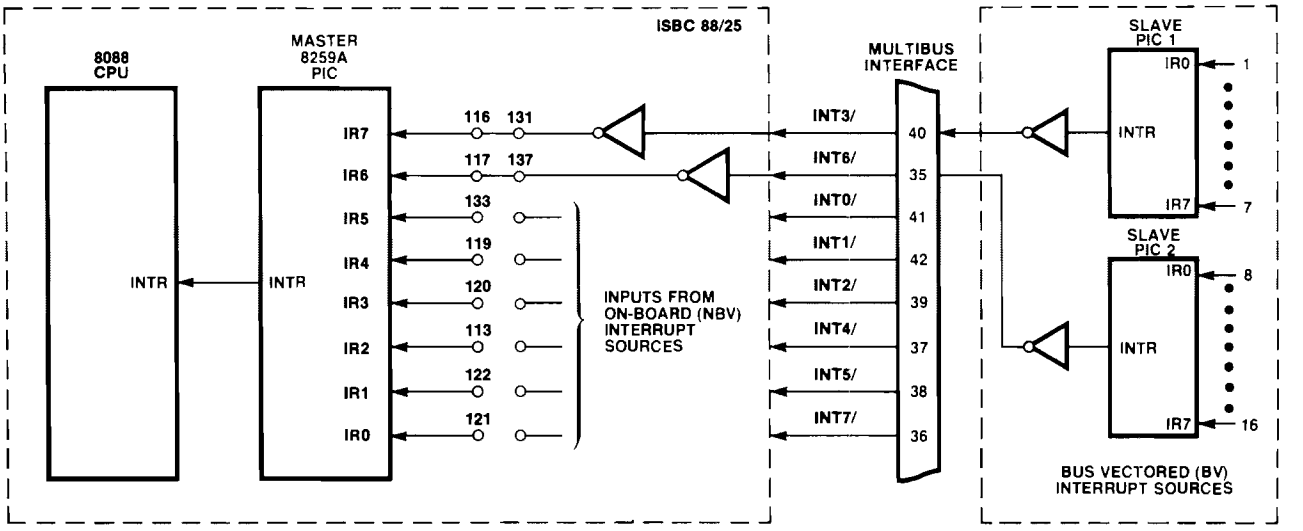


Figure 2-2. Simplified Master/Slave PIC Interconnect Example

2-20. SYSTEM CLOCK JUMPER SELECTION

The iSBC 88/25 board processor clock default connection is for 5 MHz operation. This frequency is used for all applications except the iSBC 337 Numeric Data Processor Multimodule option. When using this option, a 4.17 MHz clock frequency is required.

To implement the 4.17 MHz frequency, the following modification is required:

Remove jumper 165-166

2-21. BUS CLOCK AND CONSTANT CLOCK SELECTION

Bus Clock (BCLK/) and Constant Clock (CCLK/) are standard Multibus signals, common to most Intel iSBC boards. CCLK/ is the inverted version of BCLK/. Each signal operates at 9.83 MHz. The following table provides BCLK/ and CCLK/ jumper information:

Signal	Jumpers In	Multibus Pin
BCLK/	163-164*	P2-13
CCLK/	183-184*	P2-31

Either signal may be disabled by removing the appropriate jumper connections. Note that BCLK/ is required for Multibus arbitration operation. Only one BCLK/ source per system can be used.

2-22. WAIT STATE GENERATOR SELECTION

The iSBC 88/25 board utilizes a wait state generator to allow the 8088 processor to wait for on-board addressed devices. Wait states are generated for all PROM requests. The number of wait states for each function is jumper selectable, allowing maximum utilization of processor time according to your system configuration. Table 2-15 provides the possible jumper configurations for the wait state generator and provides the maximum address to data access times for each function.

2-23. FAILSAFE TIMER SELECTION

If non-existent off-board memory or I/O is accidentally addressed by the 8088 CPU, the iSBC 88/25 board will execute wait states indefinitely, causing the board to cease processing. An on-board failsafe timer is jumper selected to prevent this. The failsafe timer expires after a delay of approximately 10 milliseconds, giving the CPU a "fail" INT/BT signal so that it may resume processing. To enable the failsafe timer, install jumper connection 18-19. (This is a factory-installed jumper). Notice that the failsafe timer applies *only* to Multibus (off-board) requests. If you want the failsafe timer to *interrupt* processing when asserted, refer to Section 2-17 (EDGE INTR paragraph) for additional information.

Table 2-15. Wait State Generator Jumpers and Times

	Jumper	Mode	T_{ACC}	T_{CE}	T_{OE}	T_{DF}
5 Mhz	E5-E6	0 Wait	447 ns	380 ns	192 ns	130 ns
	E4-E6*	1 Waits	647 ns	580 ns	392 ns	130 ns
	E7-E6	2 Waits	847 ns	780 ns	592 ns	130 ns
4.17 MHz	E5-E6	0 Wait	567 ns	499 ns	245 ns	170 ns
	E4-E6*	1 Waits	807 ns	739 ns	485 ns	170 ns
	E7-E6	2 Waits	1047 ns	979 ns	725 ns	170 ns

NOTES:
T_{ACC} = Access Time; address to data.
T_{CE} = Chip Enable; enable signal to data.
T_{OE} = Output Enable; command to data.
T_{DF} = Data Float; data after command release.
*Factory default.

2-24. MULTIBUS INTERFACE ARBITRATION

The 8289 Bus Arbiter operates in conjunction with the 8288 Bus controller to interface the 8088 processor to the multibus interface. The 8289 Bus Arbiter can operate in several modes, depending on how it is jumper wired and the status of Common Bus Request (CBRQ/).

BCLK/ is required for proper arbitration operation.

Common Bus Request. Common Bus Request (CBRQ/), a bidirectional Multibus interface signal, allows a bus master to retain control of the system bus without contending for it each transfer cycle, as long as no other master is requesting control of the bus. A bus master requesting control of the bus, but not currently controlling it, asserts CBRQ/. This causes the controlling bus master to relinquish control of the bus when the proper surrender conditions exist. (See Table 2-16 for surrender conditions).

The CBRQ/ pins of all the bus master devices that support CBRQ/ are connected together on the iSBC modular backplane. When a bus master needs a bus resource, it informs the other bus masters that it is requesting the bus by activating CBRQ/ or BREQ/, and deactivating BPRO/. When the controlling master releases the bus, the bus exchange operates the same as described in Section 4-14.

CBRQ/ improves bus access time by allowing a bus master to retain control without contending for it each transfer cycle, as long as no other master is requesting control of the bus.

There are typically two priority resolution schemes used on the system bus: Serial and parallel. When common bus request is used, it operates identically in parallel and serial priority resolution schemes.

Any Request. The 8289 Bus Arbiter has a jumper option (ANYRQST) that controls, in conjunction with BPRN/ and CBRQ/, under what conditions the Multibus interface will be surrendered. The following paragraphs describe this option.

When ANYRQST is jumpered to a low level (161-162), the bus arbiter that was in control of the Multibus interface will retain control unless one of the following conditions exist.

1. A higher priority bus master requests the Multibus interface (as indicated by the BPRN/ signal going high.
2. The next transfer cycle of the iSBC 88/25 board does not require the use of the Multibus interface, and CBRQ/ is low.

When ANYRQST is jumpered to a high level (160-161), it permits the Multibus interface to be surrendered to a higher or lower priority bus master as though it were a bus master of high priority. A lower priority master indicates it is requesting the Multibus interface by activating CBRQ/. When this option is used, the bus master that is in control will surrender the bus as soon as possible.

If the CBRQ/ pin on the 8289 Bus Arbiter is jumpered to ground (168-169) removing it from the Multibus interface, and ANYRQST is jumpered to a high level (160-161), the Multibus interface is surrendered after each transfer cycle.

2-25. BOARD PRIORITY RESOLUTION

Your iSBC 88/25 board has been designed as a "full master" board. This means the board is equipped with bus arbitration logic and can acquire and relinquish control of the common system Multibus lines (see Section 4-14). In order for this system to be effective, a board priority scheme should be established in your system.

If your iSBC 88/25 board is the only master in the system, you must place it in the top cardcage slot (slot J2) or in a slot which has BPRN/ grounded. Normally, pin 15 (BPRN/) of the iSBC 604 backplane is grounded with a jumper between wirewrap posts B and N. (However, this connection should be

Table 2-16. 8289 Bus Arbiter Jumper Configurations

Configuration Number	Jumper Conn	CBRQ/	ANYRQST	Description
1		Low	Low	The Bus Arbiter that has control of the Multibus interface will retain control unless a higher priority master activates CBRQ/ or if the next machine cycle does not require the use of the Multibus interface it will be relinquished to a lower priority device.
	167 - 168 161 - 162	High	Low	The Bus Arbiter that has control of the Multibus interface, retains control until another Bus Arbiter pulls CBRQ/ low. When CBRQ/ goes low, the conditions are as described above.
2	167 - 168	Low	High	The Bus Arbiter that has control of the Multibus interface will surrender control to the Bus Arbiter that is pulling CBRQ/ low, regardless of its priority, upon completion of the current bus cycle.
	160 - 161	High	High	The Bus Arbiter that has control of the Multibus interface, retains control until another Bus Arbiter pulls CBRQ/ low. When CBRQ/ goes low, the conditions are as described above.
3	168 - 169* 160 - 161*	Low	High	The Bus Arbiter that has control of the Multibus interface will surrender the use of the Multibus interface after each transfer cycle.

*Factory default wiring.

verified if the factory configuration has been modified.) In this configuration, the remaining three slots can be used for any expansion boards or for lower priority master boards.

If your system includes more than one master board (CPU board), you must establish a board priority scheme. There are two methods of priority resolution available: Serial and parallel. These are described in Sections 2-26 and 2-27.

Another important consideration in setting up a multimaster system is the Multibus clock signal source. You must ensure only one of the master board is supplying the BCLK/ and CCLK/ signals to the Multibus lines. All master boards have provisions for disabling the output of these two signals (i.e., preventing the signals from going off-board). This iSBC 88/25 board BCLK/ and CCLK/ signals can be disabled by removing jumper connections. Refer to Section 2-11 for this information.

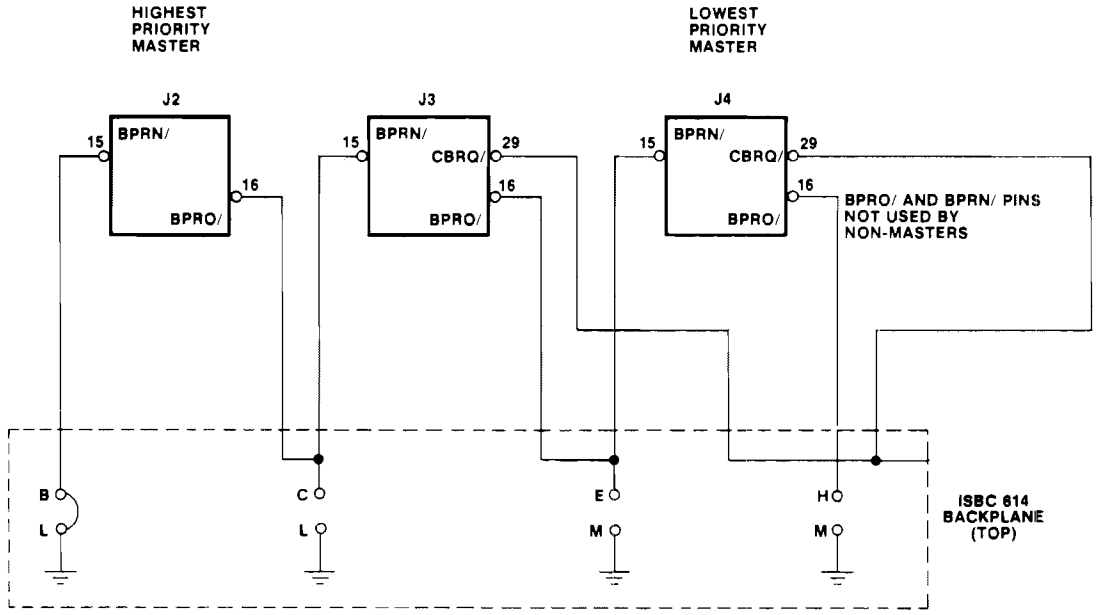
2-26. SERIAL PRIORITY RESOLUTION

Serial priority is implemented by board placement. If your iSBC 88/25 board resides in slot J2, as previously described, the next lower priority will be assigned to slot J3. Slot J4 will have the lowest priority in this scheme. Due to the propagation delay of the BPRO/ signal path, this scheme is limited to a maximum of three master boards. In the configuration shown in Figure 2-3, the master board installed in slot J2 has the highest priority and is able to acquire control of the Multibus lines anytime the bus is not busy. This is because the BPRN/ input is always true (tied to ground via jumper connection B-N on the backplane).

If the master board in slot J2 desires control of the Multibus lines, it drives its BPRO/ output high (false) and inhibits the BPRN/ inputs to the remaining lower priority master boards. The master board then takes control of the Multibus lines when the current bus cycle is completed. When finished using the Multibus lines, the J2 master board pulls its BPRO/ output low (true) and gives the J3 master board the opportunity to acquire Multibus line control. If the J3 master board does not want the Multibus lines, it pulls its BPRO/ output low (true) and gives the J4 master board the opportunity to issue control of the Multibus lines.

Stacked Chassis

If your system uses multiple stacked chassis, the jumper between posts B and N should be removed and placed between posts B and L on the top slot of the uppermost expansion backplane. This will ground BPRN/ as described above. Install the highest priority master in the uppermost slot.



NOTE: All non CBRQ/ devices must have higher priority. If a non CBRQ/ device is placed at a lower priority, it will not be able to gain control of the Multibus interface.

Top Backplane In Stacked System

Figure 2-3. Serial Priority Resolution Scheme

2-27. PARALLEL PRIORITY RESOLUTION

A parallel priority resolution scheme allows up to 16 bus masters in a single system to acquire and control the Multibus lines. Figure 2-4 illustrates one method of implementing such a scheme for resolving bus contention in a system using eight bus masters. Notice that the two highest and two lowest priority bus masters are shown installed in the master chassis. The other masters in this example are installed in the expansion chassis.

In the scheme shown in Figure 2-6, the priority encoder is a Texas Instruments 74148 device, and the priority decoder is an Intel 8205 or TI 74S138 device. Input connections to the priority encoder determine the bus priority, with input 7 having the highest priority and input 0 having the lowest priority. In Figure 2-4, the master board J3 has the highest priority, and the master board in J5 has the lowest priority.

NOTE

In a parallel priority resolution scheme, the BPRO/ output must be disabled on all master boards. Refer to the appropriate hardware reference manual for instructions.

2-28. CONNECTOR INFORMATION

For system applications the iSBC 88/25 board is designed for installation into a standard Intel Multibus cardcage assembly such as the iSBC 604 Cardcage or the iSBC 614 Expansion Cardcage. For custom applications the board may be interfaced to the other hardware by means of separately purchased Multibus compatible connectors. Table 2-17 lists recommended suppliers for such connectors.

Parallel and serial I/O connector information is also supplied in Table 2-17. For related information on parallel I/O and serial I/O cabling, refer to Sections 2-32 and 2-33.

2-29. MULTIBUS SIGNAL CHARACTERISTICS

Multibus connector P1 and auxiliary connector P2 interface the iSBC 88/25 board signals and power lines to the other boards in your system and the power supply. Where applicable, these signals conform to the Intel Multibus Interface standard. Pin assignments for P1 and P2 are listed in Tables 2-18 and 2-19 respectively. Signal definitions are provided in Table 2-20.

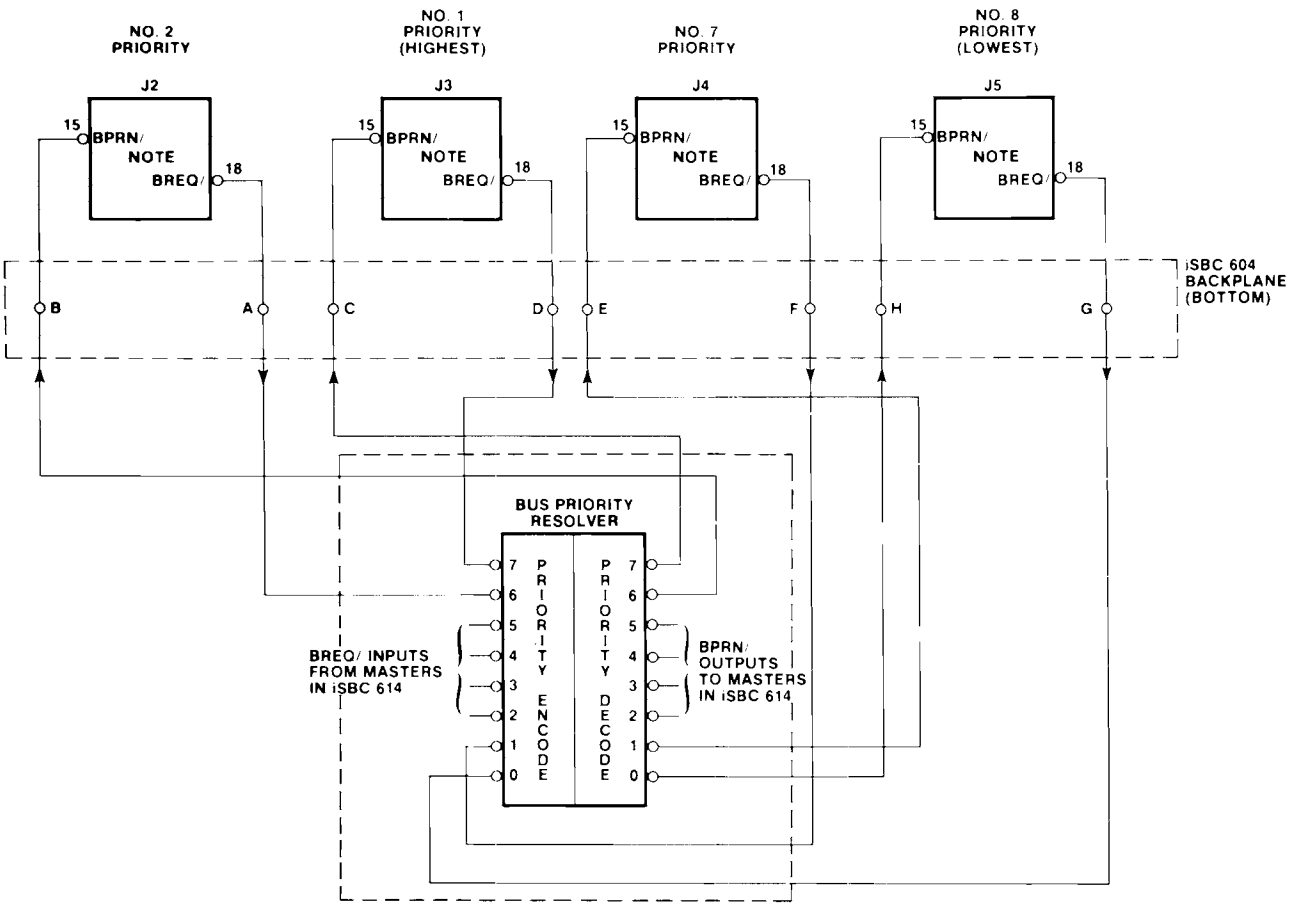
P2 signals definitions are provided in Table 2-21. Board AC characteristics are listed in Table 2-24 and shown in Figure 2-5. Board DC characteristics are listed in Table 2-22 and 2-23.

The signal names indicate whether or not the signal lines on the MULTIBUS are active high or active low. If the signal name ends with a slash ("/"), then the logical-electrical state relationship for that signal is:

Logical State	Electrical Signal Level	At Receiver	At Driver
0	H = TTL high state	5.25V≥H≥2.0V	5.25V≥H≥2.4V
1	L = TTL low state	.8V≥L≥-.5V	.5V≥L≥0V

If the signal name has no slash (no "/"), then the logical-electrical state relationship for that signal is:

Logical State	Electrical Signal Level	At Receiver	At Driver
0	L = TTL low state	.8V≥L≥.5V	.5V≥L≥0V
1	H = TTL high state	5.25V≥H≥2.0V	5.25V≥H≥2.4V



*Note: The user must implement logic, wire to mother board, and provide mounting.

Figure 2-4. Parallel Priority Resolution Scheme

These specifications are based on TTL where the power source is 5 volts ± 5%, referenced to logic ground (GND).

AC characteristics of the iSBC 88/25 board are provided in Table 2-24. Refer to the board timing diagram (Figure 2-5) for parameter identification.

Table 2-17. User Furnished Connector Details

Function	# of Pins	Centers (Inches)	Connector Type	Vendor	Vendor Part No.	Intel Part No.
Parallel I/O Connector J1	25/50	0.1000	Flat Crimp	3M 3M AMP ANSLEY SAE	3415-0001 W/ears 3415-0000 W/ears 88083-1 609-5015 S06750 Series	102211-003 N/A
			Soldered Pierced tail	GTE SYLVANIA MASTERITE MICRO PLASTICS VIKING	6AD01-25-1A1-DD NDD8GR25-DR-H-X MP-0100-25-DP-1 3KH25/9JN5	102237-001
			Wire Wrap	VIKING TI ITT CANNON	3KH25/JND5 H421011-25 EC4A050A1A	N/A
Serial I/O Connector J2	13/26	0.100	PCB Soldered Mounting Holes	AMP EDAC	1-583715-1 345-026-520-202	102233-001
			Flat Crimp	3M AMP	3462-0001 88373-5	102210-001
			Soldered Pierced Tail	EDAC	345-026-500-201	N/A
			Wire Wrap	EDAC	345-026-540-201	N/A
iSBX Multi-Module Connector J3/J4	36	0.100	Soldered PCB	VIKING	292-001	iSBC 960-5
Multibus Connector (P1)	43/86	0.156	Soldered PCB Mount	ELFAB VIKING	BS1562043PBB 2KH43/9AMK12	102247-001
			Wire Wrap No Ears	EDAC ELFAB	337-086-0540-201 BW1562D43PBB	102248-001
			Wire Wrap With .128 Dia. Mounting Holes	EDAC ELFAB	337-086-540-202 BW1562A43PBB	102273-001
Auxiliary Connector (P2)	30/60	0.100	Wire Wrap	EDAC ELFAB	345-060-524-802 BS1020A30PBB	102238-001
			With .128 Dia. Mounting Holes	TI VIKING	H421121-30 3KH30/9JNK	
			Wire Wrap No Ear	EDAC ELFAB	345-060-540-201 BW1020D30PBB	102241-001

NOTES:
1. Connector heights are not guaranteed to conform to OEM packaging equipment.
2. Wirewrap pin lengths are not guaranteed to conform to OEM packaging equipment.
3. Connector numbering convention may not agree with board connector numbers.

Table 2-18. Multibus™ Interface Connector P1 Pin Assignments

	(COMPONENT SIDE)			(CIRCUIT SIDE)		
	PIN[1]	MNEMONIC	DESCRIPTION	PIN[1]	MNEMONIC	DESCRIPTION
POWER SUPPLIES	1	GND	Signal GND	2	GND	Signal GND
	3	+5V	+5Vdc	4	+5V	+5Vdc
	5	+5V	+5Vdc	6	+5V	+5Vdc
	7	+12V	+12Vdc	8	+12V	+12Vdc
	9	-5V	-5Vdc[2]	10	-5V	-5Vdc[2]
	11	GND	Signal GND	12	GND	Signal GND
BUS CONTROLS	13	BCLK/	Bus Clock	14	INIT/	Initialize
	15	BPRN/	Bus Priority In	16	BPRO/	Bus Priority Out
	17	BUSY/	Bus Busy	18	BREQ/	Bus Request
	19	MRDC/	Mem Read Cmd	20	MWTC/	Mem Write Cmd
	21	IORC/	I/O Read Cmd	22	IOWC/	I/O Write Cmd
	23	XACK/	XFER Acknowledge	24	INH1/	Inhibit RAM[2]
BUS CONTROLS AND ADDRESS	25	LOCK/	Dual Port Lock[2]	26	INH2/	Inhibit ROM[2]
	27	BHEN/	Byte High Enable[2]	28	AD10/	
	29	CBRQ/	Common Bus Request	30	AD11/	Address
	31	CCLK/	Constant Clk	32	AD12/	Bus
	33	INTA/	Interrupt Acknowledge	34	AD13/	
INTERRUPTS	35	INT6/	Parallel	36	INT7/	Parallel
	37	INT4/	Interrupt	38	INT5/	Interrupt
	39	INT2/	Requests	40	INT3/	Requests
	41	INT0/		42	INT1/	
ADDRESS	43	ADRE/		44	ADRF/	
	45	ADRC/		46	ADRD/	
	47	ADRA/	Address	48	ADRB/	Address
	49	ADR8/	Bus	50	ADR9/	Bus
	51	ADR6/		52	ADR7/	
	53	ADR4/		54	ADR5/	
	55	ADR2/		56	ADR3/	
	57	ADR0/		58	ADR1/	
DATA	59	DATE/[2]		60	DATF/[2]	
	61	DATC/[2]		62	DATD/[2]	
	63	DATA/[2]		64	DATB/[2]	
	65	DAT8/[2]	Data	66	DAT9/[2]	Data
	67	DAT6/	Bus	68	DAT7/	Bus
	69	DAT4/		70	DAT5/	
	71	DAT2/		72	DAT3/	
	73	DAT0/		74	DAT1/	
POWER SUPPLIES	75	GND	Signal GND	76	GND	Signal GND
	77	—	Reserved	78	—	Reserved
	79	-12V	-12Vdc	80	-12V	-12Vdc
	81	+5V	+5Vdc	82	+5V	+5Vdc
	83	+5V	+5Vdc	84	+5V	+5Vdc
	85	GND	Signal GND	86	GND	Signal GND

1. All odd-numbered pins (1, 3, 5 . . . 85) are on component side of the board. Pin 1 is the left-most pin when viewed from the component side of the board with the extractors at the top. All unassigned pins are reserved.
2. Not Used on the iSBC 88/25 board.

Table 2-19. Connector P2 Pin Assignments

Pin Assignment	Signal Mnemonic	Description
P2-1, 2 P2-21, 22	Signal GND	Battery Ground
P2-3 P2-4	+5V AUX	Battery +5V Power Input
P2-6	Reserved	Reserved
P2-17	PFSN/	Power Fail Sense
P2-19	PFIN/	Power Fail Interrupt
P2-20	MPRO/	Memory Protect
P2-31	PLC	Power Line Clock
P2-32	ALE	Bus Master ALE
P2-36	BD RESET/	Board Only Reset
P2-38	AUX RESET/	System Reset Switch Input

Table 2-20. Multibus™ Interface Signal Functions

Signal	Functional Description
ADR0/-ADRF/ ADR10/-ADR13/	*Address.* These 20 lines transmit the address of the memory location or I/O port to be accessed. ADR13/ is the most significant address bit.
BCLK/	*Bus Clock.* Used to synchronize the bus contention logic on all bus masters. When generated by the iSBC 88/25 board, BCLK/ has a period of 101.7 nanoseconds (9.83 MHz) with a 35-65 percent duty cycle.
BPRN/	*Bus Priority In.* Indicates to a particular bus master that no higher priority bus master is requesting use of the bus. BPRN/ is synchronized with BCLK/.
BPRO/	*Bus Priority Out.* In serial (daisy chain) priority resolution schemes, BPRO/ must be connected to the BPRN/ input of the bus master with the next lower bus priority.
BREQ/	*Bus Request.* In parallel priority resolution schemes, BREQ/ indicates that a particular bus master requires control of the bus for one or more data transfers. BREQ/ is synchronized with BCLK/.
BUSY/	*Bus Busy.* Indicates that the bus is in use and prevents all other bus masters from gaining control of the bus. BUSY/ is synchronized with BCLK/.
CBRQ/	*Common Bus Request.* Indicates that a bus master wishes control of the bus but does not presently have control. As soon as control of the bus is obtained, the requesting bus controller raises the CBRQ/ signal.
CCLK/	*Constant Clock.* Provides a clock signal of constant frequency for use by other system modules. When generated by the iSBC 88/25 board, CCLK/ has a period of 101.7 nanoseconds (9.83 MHz) with a 35-65 percent duty cycle.
DAT0/-DAT7/	*Data.* These 8 bidirectional data lines transmit and receive data to and from the addressed memory location or I/O port. DAT7/ is the most significant bit.
LOCK/	*Dual Port RAM Lock.* Disables system dual Port RAM when asserted and jumper is installed.

Table 2-20. Multibus™ Interface Signal Functions (Continued)

Signal	Functional Description
INIT/	*Initialize.* Resets the entire system to a known internal state.
INTA/	*Interrupt Acknowledge.* This signal is issued in response to an interrupt request.
INT0/-INT7/	*Interrupt Request.* These eight lines transmit Interrupt Requests to the appropriate interrupt handler. INT0 has the highest priority.
IORC/	*I/O Read Command.* Indicates that the address of an I/O port is on the Multibus interface address lines and that the output of that port is to be read (placed) onto the Multibus interface data lines.
IOWC/	*I/O Write Command.* Indicates that the address of an I/O port is on the Multibus interface interface address lines and that the contents on the Multibus interface data lines are to be accepted by the addressed port.
MRDC/	*Memory Read Command.* Indicates that the address of a memory location is on the Multibus interface address lines and that the contents of that location are to be read (placed) on the Multibus interface data lines.
MWTC/	*Memory Write Command.* Indicates that the address of a memory location is on the Multibus interface address lines and that the contents on the Multibus interface data lines are to be written into that location.
XACK/	*Transfer Acknowledge.* Indictes that the addressed memory location has completed the specified read or write operation. That is, data has been placed onto or accepted from the Multibus interface data lines.

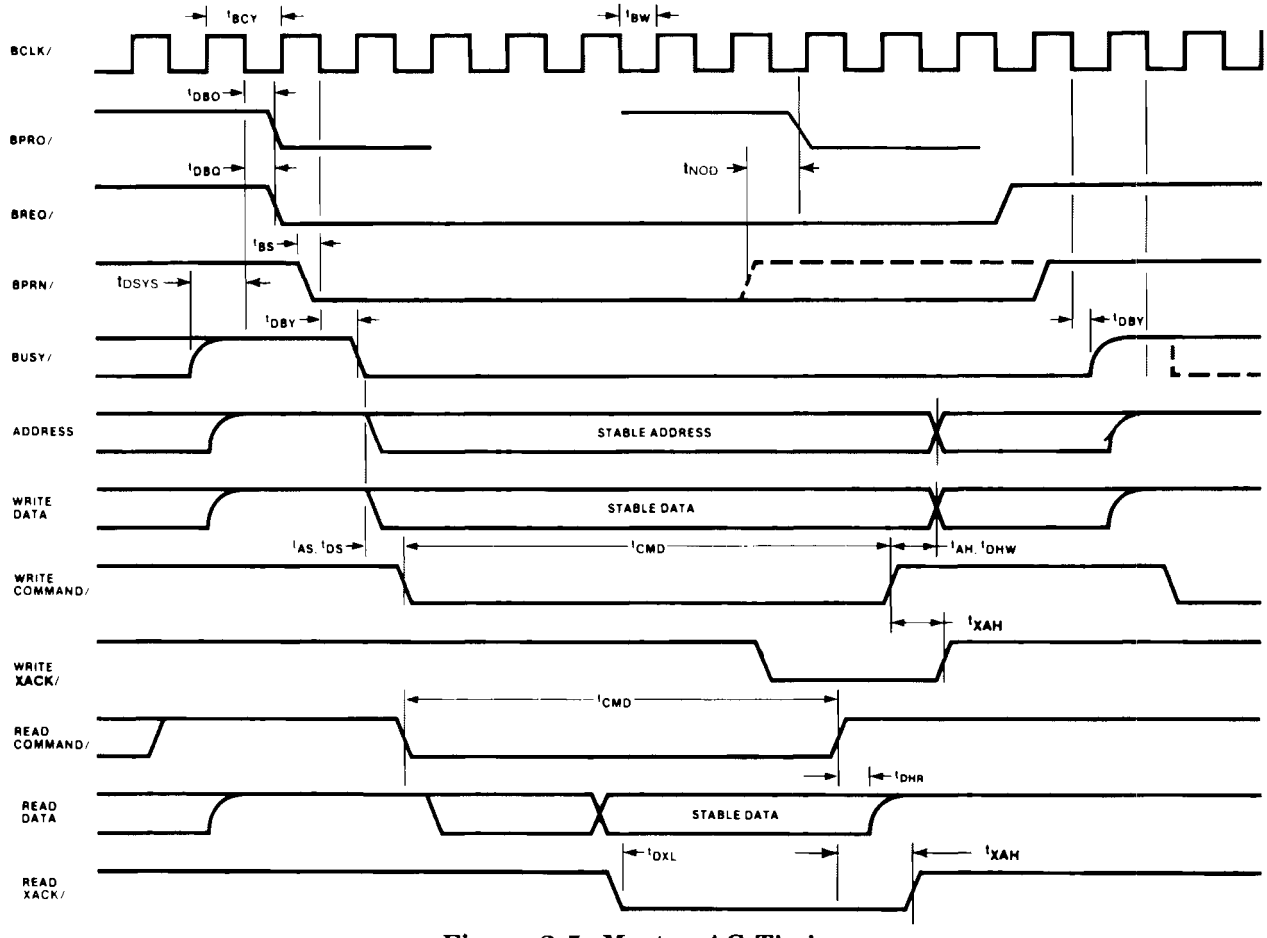


Figure 2-5. Master AC Timing

Table 2-21. P2 Signal Definitions

PFIN/	*Power Fail Interrupt.* This input from the power supply interrupts the CPU when a power failure occurs. See section 2-31.
PFSN/	*Power Fail Sense.* This line is the output of a latch which indicates a power failure has occurred. It is reset by PFSR/ and must be powered by the standby power source. See section 2-31.
MPRO/	*Memory Protect.* When true, this externally generated signal prevents access to the on-board RAM during periods of uncertain DC power. See section 2-31.
ALE	*Address Latch Enable.* Indicates the CPU is operating. Typically, this signal is used to drive a front panel RUN indicator.
BD RESET/	*Board Reset.* This signal resets the iSBC 88/25 board only. It will not reset other boards in the system.
AUX RESET/	*Auxiliary Reset.* Typically this RESET signal is generated by a front panel switch. The signal is functionally equivalent to INIT/.

Table 2-22. iSBC 88/25™ Board DC Characteristics

Signals	Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
ADR0/-ADRF/ ADR10/-ADR13/ LOCK/ LS240	V_{OL}	Output Low Voltage	I_{OL} = 24 mA		0.5	V
	V_{OH}	Output High Voltage	I_{OH} = -15	2.4		V
	I_{LH}	Output Leakage High	V_O = 2.7V		20	μA
	I_{LL}	Output Leakage Low	V_O = 0.4V		-20	μA
	*C_L	Capacitive Load			18	pF
BCLK/ S37	V_{OL}	Output Low Voltage	I_{OL} = 59.5 mA		0.5	V
	V_{OH}	Output High Voltage	I_{OH} = -3 mA	2.7		V
	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.45V		-0.5	mA
	I_{IH}	Input Current at High V	V_{IN} = 5.25V		60	μA
	*C_L	Capacitive Load			15	pF
BPRN/	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.45V		-0.5	mA
	I_{IH}	Input Current at High V	V_{IN} = 5.25V		60	μA
	*C_L	Capacitive Load			18	pF
BPRO/	V_{OL}	Output Low Voltage	I_{OL} = 10 mA		0.45	V
	V_{OH}	Output High Voltage	I_{OH} = -0.4 mA	2.4		V
	*C_L	Capacitive Load			15	pF
BREQ/	V_{OL}	Output Low Voltage	I_{OL} = 10 mA		0.45	V
	V_{OH}	Output High Voltage	I_{OH} = -0.4 mA	2.4		V
	*C_L	Capacitive Load			10	pF
BUSY/ CBRQ/, INTROUT/ 7406 (OPEN COLLECTOR)	V_{OL}	Output Low Voltage	I_{OL} = 20 mA		0.45	V
	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.45V		-0.5	mA
	I_{IH}	Input Current at High V	V_{IN} = 5.25V		60	μA
	*C_L	Capacitive Load			20	pF

Table 2-22. iSBC 88/25™ Board DC Characteristics (Continued)

Signals	Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
CCLK/	V_{OL}	Output Low Voltage	I_{OL} = 60 mA		0.5	V
	V_{OH}	Output High Voltage	I_{OL} = -3 mA	2.7		V
	*C_L	Capacitive Load			15	pF
DAT0/-DATF/	V_{OL}	Output Low Voltage	I_{OL} = 32 mA		0.45	V
	V_{OH}	Output High Voltage	I_{OH} = -5 mA	2.4		V
	V_{IL}	Input Low Voltage			0.9	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.45V		-0.20	mA
	I_{LH}	Output Leakage High	V_O = 5.25V		50	μA
	*C_L	Capacitive Load			18	pF
INIT/ (SYSTEM RESET) 7406 & LS00	V_{OL}	Output Low Voltage	I_{OL} = 39 mA		0.4	V
	V_{OH}	Output High Voltage	OPEN COLLECTOR			
	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	V_{IL}	Input Current at Low V	V_{IN} = 0.4V		-0.71	mA
	I_{IH}	Input Current at High V	V_{IN} = 2.4V		—.22	mA
	*C_L	Capacitive Load			15	pF
INT0/-INT7/ LS240	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Inpt Current at Low V	V_{IN} = 0.4V		-0.2	mA
	I_{IH}	Input Current at High V	V_{IN} = 2.7V		20	μA
	*C_L	Capacitive Load			18	pF
IORC/, IOWC/ MRDC/ MWTC/	V_{OL}	Output Low Voltage	I_{OL} = 32 mA		0.5	V
	V_{OH}	Output High Voltage	I_{OL} = -5 mA	2.4		V
	I_{LH}	Output Leakage High	V_O = 5.25 V		100	μA
	I_{LL}	Output Leakage Low	V_O = 0.45V		-100	μA
	*C_L	Capacitive Load			15	pF
INTA/, MRDC/, MWTC/ S32	V_{OL}	Output Low Voltage	I_{OL} = 30 mA		0.5	V
	V_{OL}	Output High Voltage	I_{OL} = -5 mA	2.4		V
	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.45V		-2.0	mA
	I_{IH}	Input Current at High V	V_{IN} = 2.7V		150	μA
	*C_L	Capacitive Load			25	pF
XACK/	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.4V		-0.4	mA
	I_{IH}	Input Current at High V	V_{IN} = 2.7V		-20	μA
	*C_L	Capacitive Load			15	pF

*Capacitive load values are approximations.

Table 2-23. Auxiliary Signal (Connector P2) DC Characteristics

Signals	Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
ALE	V_{OL}	Output Low Voltage	I_{OL} = 16 mA		0.5	V
	V_{OH}	Output High Voltage	I_{OH} = -1.0 mA	2.4		V
	*C_L	Capacitive Load			20	pF
PFIN/	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.4		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.4V		-0.4	mA
	I_{IH}	Input Current at High V	V_{IN} = 2.4V		20	μ
	*C_L	Capacitive Load			20	pF
MPRO/	V_{IL}	Input Low Voltage			0.80	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.4V		-0.91	mA
	I_{IH}	Input Current at High V	V_{IN} = 2.4V		0.31	mA
	*C_L	Capacitive Load			15	pF
AUX RESET/ BD RESET/	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.6		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.45V		-0.5	mA
	I_{IH}	Input Current at High V	V_{IN} = 5.25V		50	μA

*Capacitance load values are approximations.

Table 2-24. AC Characteristics

Parameter	Description	Minimum	Maximum	Units
t_{BCY}	Bus Clock Period	100	D.C.	ns
t_{BW}	Bus Clock Width	0.35 t_{BCY}	0.65 t_{BCY} (not restricted)	
t_{AS}	Address Set-Up Time (at Slave Board)	85		
t_{DS}	Write Data Set Up Time	51		ns
t_{AH}	Address Hold Time	165		ns
t_{DHW}	Write Data Hold Time	83		ns
t_{DXL}	Read Data Set Up Time to XACK	-250		ns
t_{DHR}	Read Data Hold Time	-5		ns
t_{XAH}	Acknowledge Hold Time	-210	683	ns
t_{CMD}	Command Pulse Width	400		μs
t_{INTA}	INTA/ Width	400		ns
t_{CSEP}	Command Separation	400		ns
t_{DBQ}	↓BCLK/ to BREQ Low Delay	0	35	ns
t_{DBQ}	↓BCLK/ to BREQ High Delay	0	35	ns
t_{BPNS}	BPRN/ to ↓BCLK/ Setup Time	15		ns
t_{DBY}	BUSY/ delay from ↓BCLK/	0	60	ns
t_{DSYS}	BUSY/ to ↓BCLK/ Setup Time	20		ns

Table 2-24. AC Characteristics (Continued)

Parameter	Description	Minimum	Maximum	Units
t_{DBO}	↓BCLK/ to BPRO/ (CLK to Priority Out)	0	40	ns
t_{NOD}	BPRN/ to BPRO/ (Priority In to Out)	0	25	ns
t_{CBRD}	↓BCLK/ to CBRQ/ (CLK to Common Bus Request)	0	60	ns
t_{CBRS}	CBRQ/ to ↓CBLK/ Setup Time	20		
t_{CCY}	C-clock Period	100	110	ns
t_{CW}	C-clock Width	0.35 t_{CCY}	0.65 t_{CCY}	ns
t_{INIT}	INIT/Width	5		ms

2-30. PARALLEL I/O DC CHARACTERISTICS

Parallel I/O DC characteristics of the iSBC 88/25 board are provided in Table 2-25.

2-31. POWER FAIL BATTERY BACKUP PROVISIONS

In an optional mode, the iSBC 88/25 board may be configured for battery backup operation. This means

Table 2-25. Parallel I/O DC Characteristics

Signals	Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
Port C8 Bidirectional Drivers	V_{OL}	Output Low Voltage	I_{OL} = 32 mA		0.45	V
	V_{OH}	Output High Voltage	I_{OH} = -5 mA	2.4		V
	V_{IL}	Input Low Voltage			0.9	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.45V		-5.25	mA
	*C_L	Capacitive Load			18	pF
8255A Driver/Receiver	V_{OL}	Output Low Voltage	I_{OL} = 1.7 mA		0.45	V
	V_{OH}	Output High Voltage	I_{OH} = -200 μA	2.4		V
	V_{IL}	Input Low Voltage		0.5	0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.45		10	μA
	I_{IH}	Input Current at High V	V_{IN} = 5.0		10	μA
	*C_L	Capacitive Load			18	pF
EXT INTR/	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.4V		-0.4	mA
	I_{IH}	Input Current at High V	V_{IN} = 2.7V		20	μA
	*C_L	Capacitive Load			30	pF

*Capacitive load values are approximations.

you may have a battery connected to the board, which is used to preserve memory during an AC power failure. In order for the battery backup scheme to function, your power supply must provide the following signals:

a. PFIN/ *Power Fail Interrupt.* Asserted at least 8 milliseconds before DC voltages are lost.

b. MPRO/ *Memory Protect.* Asserted at least 50 microseconds before DC voltages are lost.

c. PFSN/ *Power Fail Sense.* The output of an external, battery powered latch which indicates a power failures has occurred.

To implement a typical battery backup scheme on the iSBC 88/25 board, the following connections are required:

a. Connect +5 Volt battery positive leads to auxiliary connector pins P2-3 and P2-4.

b. Connect battery return lead to auxiliary connector pins P2-1 and P2-2.

c. Remove jumper connection 158-159.

d. Connect power supply PFIN/ line to auxiliary connector P2-19.

e. Remove jumper 109-110 and install jumper 107-109. This routes the PFIN/ input to the 8088 NMI input.

f. Install a jumper between parallel port matrix post 24 (NMI mask) and the desired port CC output bit.

g. Connect power supply MPRO/ line to auxiliary connector P2-20.

h. Connect the PFSN/ line to auxiliary connector P2-17. PFSN/ is the output of the external, battery powered latch which indicates that a power failure has occurred. This latch is reset by PFSR/, which can be implemented with an unused port CC bit.

In this typical battery backup configuration, if a power failure occurs, the power supply asserts PFIN/ which in turn initiates the NMI interrupt. This causes your power fail interrupt software routine to be executed. The preinterrupt conditions must be stored in protected memory during this routine. Contents of internal registers should be stored in RAM, which is then locked up when MPRO/ is asserted. When power is restored, the PFSN/ signal is read by the parallel port, indicating a power failure has occurred. Your power on routine could then read contents of RAM before executing, thereby minimizing data loss.

2-32. PARALLEL I/O CABLING

Parallel I/O ports C8, CA, and CC are controlled by the 8255A-5 Parallel Peripheral Interface (PPI) device are connected to external equipment via edge connector J1. Pin assignments for edge connector J1 are provided in Table 2-26. Bit order for port CC may be altered by jumper connection. Refer to Section 2-17 for instructions.

Table 2-26. Parallel I/O Connector J1 Pin Assignments

Pin[1,2]	Function	Pin[1,2]	Function
1	Ground	2	Port CA bit 7
3	↑	4	Port CA bit 6
5		6	Port CA bit 5
7		8	Port CA bit 4
9		10	Port CA bit 3
11		12	Port CA bit 2
13		14	Port CA bit 1
15	Ground	16	Port CA bit 0
17	Ground	18	Port CC bit 3
19	↑	20	Port CC bit 2
21		22	Port CC bit 1
23		24	Port CC bit 0
25		26	Port CC bit 4
27		28	Port CC bit 5
29		30	Port CC bit 6
31	Ground	32	Port CC bit 7
33	Ground	34	Port C8 bit 7
35	↑	36	Port C8 bit 6
37		38	Port C8 bit 5
39		40	Port C8 bit 4
41		42	Port C8 bit 3
43		44	Port C8 bit 2
45		46	Port C8 bit 1
47	Ground	48	Port C8 bit 0
49	Ground	50	EXT INTR0/

1. All odd-numbered pins 1, 3, 5, ... 49) are on component side of board. Pin 1 is the right-most pin when viewed from the component side of the board with the extractors at the top.
2. Cable connector numbering convention may not agree with board connector numbering convention.

DC characteristics of the parallel I/O port lines are listed in Table 2-25. Connector information for edge connector J1 is provided in Table 2-17.

For maximum reliability, the transmission path from the I/O source to the iSBC 88/25 board should be limited to a maximum of 3 meters (10 feet). Recommended bulk cable types are provided in Table 2-27.

Table 2-27. Bulk Cable Types

Flat cable, 50 conductor w/o ground plane	3M 3306-50
Flat cable, 50 conductor with ground plane	3M 3380-50
Woven cable, 25 pair	3M 3321-25

2-33. SERIAL I/O CABLING

Pin assignments and signal names for the serial I/O port interface connector (J2) are listed in Table 2-28. An Intel iSBC 955 Cable Set is recommended for RS 232C interfacing. One cable assembly consists of a 25 conductor flat cable with a 26-pin connector at one end and an RS 232C interface connector at the other end. A second cable assembly is included in the iSBC 955 set, which consists of an RS 232C connector on one end and spade lugs on the other end. The spade lugs are used to connect the cable to a teletypewriter.

For custom applications where cables will be made for the iSBC 88/25 board, it is important to note that the mating connector for J2 has 26 pins, whereas the RS 232C connectors has 25 pins. Consequently, when connecting the 26-pin mating connector to 25-connector flat cable, be sure that the cable makes contact with pins 1 and 2 of the mating connector and not pin 26. Table 2-29 provides pin correspondence between connector J2 and the RS 232C connector. When attaching the connector to J2 be sure that the PC connector is oriented properly with respect to pin 1 on the board. Refer to the footnote at the bottom of Table 2-28.

Table 2-28. Connector J2 Pin Assignments

Pin No.	iSBC 88/25 Signal	PCI Function
J2 - 1	Not Used	—
J2 - 2	Ground	GND
J2 - 3	Not Used	—
J2 - 4	Transmitted Data	RxD Input
J2 - 5	See J2 - 26	See J2 - 26
J2 - 6	Received Data	TxD Output
J2 - 7	External Clock	TxC/RxC Input
J2 - 8	Request To Send	CTS/ Input
J2 - 9	Not Used	—
J2 - 10	Clear To Send	RTS/ Output
J2 - 11	Not Used	—
J2 - 12	Data Set Ready	DSR/ Input
J2 - 13	Data Terminal Ready	DTR/ Output
J2 - 14	Ground	GND
J2 - 15	Not Used	—
J2 - 16	Not Used	—
J2 - 17	Not Used	—
J2 - 18	Not Used	—
J2 - 19	-12 Vdc[3]	—
J2 - 20	Not Used	—
J2 - 21	See J2 - 26[3]	See J2 - 26
J2 - 22	+12 Vdc[3]	—
J2 - 23	+5 Vdc[3]	—
J2 - 24	Not Used	—
J2 - 25	Ground	GND
J2 - 26	Secondary TxD or Clock Out[3]	STxD or TxC/TxD

Notes:

1. Odd numbered pins are on component side of board; even pins on solder side.
2. Cable connector numbering convention may not correspond with J2 numbering.
3. Not connected at factory.

Table 2-29. RS232 Signals Pin Correspondence

PC Conn. J2	RS232C Conn.	PC Conn. J2	RS232C Conn.
1	14	14	7
2	1	15	21
3	15	16	8
4	2	17	22
5	16	18	9
6	3	19	23
7	17	20	10
8	4	21	24
9	18	22	11
10	5	23	25
11	19	24	12
12	6	25	N/C
13	20	26	13

2-34. MULTIMODULE BOARDS AND THE iSBX BUS

The iSBC 88/25 board is equipped with two 8-bit iSBX (single board expansion) bus connectors (J3 and J4). This bus allows on-board I/O expansion, using optional iSBX Multimodule boards. These boards should not be confused with the optional RAM and ROM/PROM expansion boards which are interfaced to the on-board memory bus. Connectors J3 and J4 may be used only for iSBX Multimodule boards.

Table 2-30 provides the iSBX bus connector pin assignments, and Table 2-31 provides signal descrip tions. Each of the two connectors has identical pin assignments and physical layout.

For installation instructions, refer to the specific iSBX Multimodule board hardware reference manual.

When a Multimodule board is installed, the iSBC 88/25 board's power requirements will increase by the amount specified in the Multimodule board reference manual.

Table 2-30. iSBX™ Bus Connector Pin Assignments

Pin	Mnemonic	Description	Pin	Mnemonic	Description
35	GND	SIGNAL GROUND	36	+5V	+5 Volts
33	MD0	MDATA BIT 0	34	—	RESERVED
31	MD1	MDATA BIT 1	32	—	RESERVED
29	MD2	MDATA BIT 2	30	OPT0	OPTION 0
27	MD3	MDATA BIT 3	28	OPT1	OPTION 1
25	MD4	MDATA BIT 4	26	—	RESERVED
23	MD5	MDATA BIT 5	24	—	RESERVED
21	MD6	MDATA BIT 6	22	MCS0/	M CHIP SELECT 0
19	MD7	MDATA BIT 7	20	MCS1/	M CHIP SELECT 1
17	GND	SIGNAL GROUND	18	+5V	+5 Volts
15	IORD/	IO READ COMMAND	16	MWAIT/	M WAIT
13	IOWRT/	IO WRITE COMMAND	14	MINTR0	M INTERRUPT 0
11	MA0	M ADDRESS 0	12	MINTR1	M INTERRUPT 1
9	MA1	M ADDRESS 1	10	—	RESERVED
7	MA2	M ADDRESS 2	8	MPST/	M PRESENT
5	MRESET	M RESET	6	MCLK	M CLOCK
3	GND	SIGNAL GROUND	4	+5V	+5 Volts
1	+12V	+12 Volts	2	-12V	-12 Volts

Table 2-31. iSBX™ Bus Signal Descriptions

IORD/	Commands the Multimodule board to perform the read operation.
IOWRT/	Commands the Multimodule board to perform the write operation.
MRESET/	Initializes the Multimodule board to a known internal state.
MCS0/	Chip select. Selects even only I/O addresses (80-8F) on the J3 Multimodule board and even only addresses (A0-AF) on the J4 Multimodule board.
MCS1/	Chip select. Selects even only I/O addresses (90-9F) on the J3 Multimodule board and even only addresses (B0-BF) on the J4 Multimodule board.
MA 0-2	Least three bits of the I/O address. Used in conjunction with the chips select and command lines.
MPST/	Multimodule present indicator. Informs iSBC 88/25 board that a Multimodule board(s) is installed.
MINTR0-1	Interrupt request lines from the Multimodule board to the iSBC 88/25 board interrupt matrix.
MWAIT/	Causes iSBC 88/25 board to execute wait states until Multimodule board is ready to respond.
MCLK/	9.83 MHz Multimodule board timing reference from iSBC 88/25 board.
OPT0-1	Optional use lines. May be used for additional interrupt request lines, or connected to PPI interface.
MD0-7	Bidirectional data lines.

2-35. FINAL INSTALLATION

CAUTION

Always turn off the system power supply before installing or removing the iSBC 88/25 board from its system, or before installing or removing any I/O cables. Failure to observe these precautions may result in damage to the board.

In an iSBC Single Board Computer based system, install the iSBC 88/25 board in the cardcage slot which corresponds to your priority scheme or application. Ensure that an auxiliary connector is installed in the cardcage if any of the iSBC 88/25 board P2 signals are used in your system.

CHAPTER 3
PROGRAMMING INFORMATION

3-1. INTRODUCTION

Several Intel programmable devices reside on the iSBC 88/25 board. This chapter provides programming information for these devices and gives typical examples for most applications. Memory and I/O addressing are provided in table form, for quick reference.

3-2. MEMORY ADDRESSING

The iSBC 88/25 board may accommodate up to 64K bytes of on-board ROM. Four sockets are provided for ROM devices. The amount of on-board ROM may be doubled by adding the optional iSBC 341 ROM Expansion Module (refer to Section 2-7). Table 3-1 provides the addressing for the various ROM configurations possible on the iSBC 88/25 board.

The factory configuration for 2716 devices (2K X 8) indicates an on-board ROM address range from FE000 to FFFFF (hexadecimal). From Table 3-1 you will notice that on-board ROM addressing always ends at the highest possible address (FFFFF), regardless of size. In the maximum configuration, without the iSBC 341 Expansion Module, the address range would be from F0000 to FFFFF.

Table 3-1. On-Board ROM Addresses

Device Type & Size	Address	Total Space
2716 (2K X 8)	FE000 - FFFFF	8K
2732 (4K X 8)	FC000 - FFFFF	16K
2764 (8K X 8)	F8000 - FFFFF	32K
27840 (16K X 8)	F0000 - FFFFF	64K
ROM Addresses With iSBC 341 ROM Module		
2716 (2K X 8)	FC000 - FFFFF	16K
2732 (4K X 8)	F8000 - FFFFF	32K
2764 (8K X 8)	F0000 - FFFFF	64K
27840 (16K X 8)	E0000 - FFFFF	128K
Notes: 1. Device sizes cannot be mixed.		

[redacted] (hexadecimal). With the optional iSBC 302 RAM Expansion Module installed, RAM addressing becomes 00000-02FFF or 03FFF. [redacted]. Tables 3-2 summarizes on-board RAM addressing.

Table 3-2. On-Board RAM Addresses

Configuration	Addresses	Total Size
[redacted]	[redacted]	[redacted]
With iSBC 302, part	0 - 02FFF	12K bytes
With iSBC 302, full	0 - 03FFF	16K bytes

[redacted] For failsafe timer jumper information, refer to Section 2-20.

When the CPU is addressing on-board memory, an internal PROM or RAM Acknowledge signal is automatically generated to prevent unnecessary wait states. When the CPU is addressing off-board system memory via the Multibus lines, the CPU must first gain control of the Multibus lines and, after the Memory Read or Memory Write command is given, it will execute wait states until a Transfer Acknowledge signal is received from the addressed memory.

3-3. I/O ADDRESSING

The on-board 8088 CPU communicates with the programmable devices through a sequence of I/O read and I/O write commands. Each device has a specific fixed (dedicated) address, or group of addresses, through which commands and/or data are issued or accepted. All of these fixed on-board I/O addresses are listed in Table 3-3. In addition to the board's programmable I/O devices, certain other functions have specific addresses assigned to them. These addresses are also included in the table.

3-4. SYSTEM INITIALIZATION

When power is initially applied to the board, the reset signal (RESET) is automatically generated by the 8284A Clock Generator/Driver. This clears the 8088 internal counters, instruction registers, and the interrupt enable circuitry. The first instruction is then executed from memory location FFFF0. This location should contain a JMP instruction which directs the processor to the actual program beginning.

Table 3-3. I/O Port Addresses

Address*	Device	Input Function	Output Function
C0 or C4	8259A PIC	ICW1/OCW2/OCW3	Status & Poll
C2 or C6	8259A PIC	ICW2/ICW3/ICW4/OCW1 Mask	OCW1 Mask
C8	8255A PPI	Port A	Port A
CA	8255A PPI	Port B	Port B
CC	8255A PPI	Port C	Port C
CE	8255A PPI	Control Word	None
D0	8253 PIT	Counter 0	Counter 0
D2	8253 PIT	Counter 1	Counter 1
D4	8253 PIT	Counter 2	Counter 2
D6	8253 PIT	Control Word	None
D8 or DC	8251A PCI	Data	Data
DA or DE	8251A PCI	Mode or Command Word	Status

* Odd I/O Port Addresses are reserved.

iSBX™ Multimodule Connector I/O Port Addresses

Addresses	Connector	Mode	Select	Description
A0 A2 A4 A6 A8 AA AC AE	J4	8-bit	MCS0/	SBX 1 CS0/
B0 B2 B4 B6 B8 BA BC BE	J4	8-bit	MCS1/	SBX 1 CS1/
80 82 84 86 88 8A 8C 8E	J3	8-bit	MCS0/	SBX 2 CS0/
90 92 94 96 98 9A 9C 9E	J3	8-bit	MCS1/	SBX 2 CS1/

The RESET signal also is routed to all other iSBC boards in your system (as INIT/) via Multibus line P1-P14. On-board, the RESET signal is routed to the 8255A parallel interface, the 8251A serial interface, the interrupt acknowledge circuitry, and the iSBX connectors. The RESET signal causes:

a. The 8251A serial interface device to idle and wait for a set of command words; and

b. Sets the 8255A parallel ports to mode 0, input.

The reset/initialize signal can also be generated by an auxiliary reset switch, such as on a system front panel. This switch should be connected to P2 - 38 (AUX RESET/) on the auxiliary connector.

Another switch may be used to generate an on-board only RESET. This switch should be connected to P2 - 36 (BD RESET/) on the auxiliary connector.

3-5. 8253 PIT PROGRAMMING

Two frequencies are input to the 8253 PIT (CLK0 and CLK2 = 1.228 MHz; CLK2 = 153.6 KHz). The default (factory connected) and optional jumpers for selecting the clock inputs to the three counters are listed in Table 2-7. Jumpers are included so that counters 0, 1 and 2 can provide real time interrupts to the 8259A PIC.

Before programming the 8253A PIT, ascertain the input clock and output function of each of the counters to be used. These factors are determined and established by the user during installation.

3-6. MODE CONTROL WORD AND COUNT

All three counters must be initialized prior to their use. The initialization for each counter consists of two steps:

a. A mode control word (Figure 3-1) is written to the control register for each individual counter.

b. A count number is loaded into each counter. The count number is in one or two 8-bit bytes as determined by the mode control word.

The mode control word (Figure 3-1) does the following:

a. Selects counter to be loaded.

b. Selects counter operating mode.

c. Selects one of the following four counter read/load functions:
   (1) Counter latch (for stable read operation).
   (2) Read or load most-significant byte only.
   (3) Read or load least-significant byte only.
   (4) Read or load least-significant byte first, then most-significant byte.

d. Sets counter for either binary or BCD count.

The mode control word and the count register bytes for any given counter must be entered in the following sequence:

a. Mode control word.

b. Least-significant count register byte (if programmed by mode control word).

c. Most-significant count register byte (if programmed by mode control word).

As long as the preceding procedure is followed for each counter, the chip can be programmed in any convenient sequence. For example, mode control

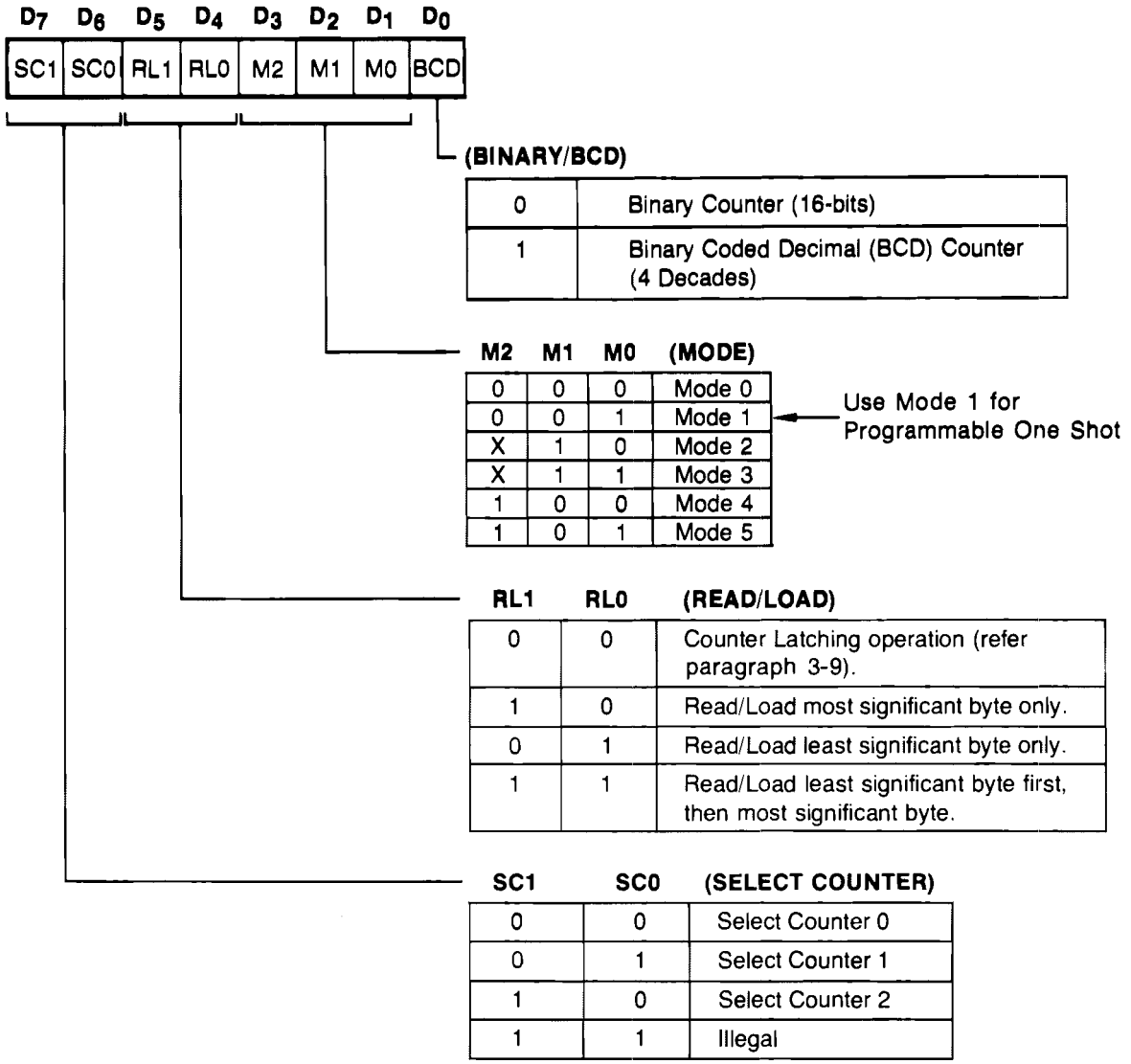


Figure 3-1. PIT Control Word Format

words can be loaded first into each of the three counters, followed by the least-significant byte, most-significant byte, etc. Figure 3-2 shows the two programming sequences described previously.

Since all counters in the PIT chip are down counters, the value loaded in the count registers is decremented. Loading all zeros into a count register results in a maximum count of 2^{16} for binary numbers or 10^4 for BCD numbers.

When a selected count register is to be loaded, it must be loaded with the number of bytes programmed in the mode control word. One or two bytes can be loaded, depending on the appropriate count. These two bytes can be programmed at any time following the mode control word, as long as the correct number of bytes is loaded in order.

The count mode selected in the control word controls the counter output. As shown in Figure 3-1, the PIT chip can operate in any of six modes:

a. Mode 0: Interrupt on terminal count. In this mode, the counters can be used for auxillary functions, such as generating real-time interrupt intervals. After the count value is loaded into the count register, the counter output goes low and remains low until the terminal count is reached. The output then goes high until the count register is reloaded or the mode is reloaded.

b. Mode 1: Programmable one-shot. In this mode, the output of the counters will go low on the count following the rising edge of the gate input. The output will go high on the terminal count. If a new count value is loaded while the output is low, it will not affect the duration of the one-shot pulse until the succeeding trigger. The current count can be read at any time without affecting the one-shot pulse. The one-shot is retriggerable, hence the output will remain low for the full count after any rising edge of the gate input.

c. Mode 2: Rate generator. In this mode, the output of the counters will be low for one period of the clock input. The period from one output pulse to the next equals the number of input counts in the count register. If the count register is reloaded between output pulses, the present period will not be affected but the subsequent period will reflect the new value. The gate input, when low, will force the output high. When the gate input goes high, the counter will start from the initial count. Thus, the gate input can be used to synchronize the counter. When mode 2 is set, the output will remain high until after the count register is loaded; thus, the count can be synchronized by software.

d. Mode 3: Square wave generator. In this mode, the counter output remains high until one-half

PROGRAMMING FORMAT

Step		
1		Mode Control Word Counter n
2	LSB	Count Register Byte Counter n
3	MSB	Count Register Byte Counter n

ALTERNATE PROGRAMMING FORMAT

Step		
1		Mode Control Word Counter 0
2		Mode Control Word Counter 1
3		Mode Control Word Counter 2
4	LSB	Counter Register Byte Counter 1
5	MSB	Count Register Byte Counter 1
6	LSB	Count Register Byte Counter 2
7	MSB	Count Register Byte Counter 2
8	LSB	Count Register Byte Counter 0
9	MSB	Count Register Byte Counter 0

Figure 3-2. PIT Programming Sequence Examples

of the count value in the count register has been decremented (for even numbers). The output then goes low for the other half of the count. If the value in the count register is odd, the counter output is high for (N + 1)/2 counts, and low for (N - 1)/2 counts.

e. Mode 4: Software triggered strobe. After this mode is set, the output will be high. When the count is loaded, the counter begins counting. On terminal count, the output will go low for one input clock period and then go high again. If the count register is reloaded between output pulses, the present count will not be affected, but the subsequent period will reflect the new value. The count will be inhibited while the gate input is low. Reloading the count

f. Mode 5: Hardware triggered strobe. The counter will start counting on the rising edge of the gate input and the output will go low for one clock period when the terminal count is reached. The counter is retriggerable. The output will not go low until the full count after the rising edge of the gate input.

Table 3-4 provides a summary of the counter operation versus the gate inputs. The gate inputs are pulled-up to a high level. These gates may optionally be controlled by port CC.

Table 3-4. PIT Counter Operation Vs. Gate Inputs

Signal Status / Modes	Low Or Going Low	Rising	High
0	Disables counting	—	Enables counting
1	—	1) Initiates counting 2) Resets output after next clock	—
2	1) Disables counting 2) Sets output immediately high	Initiates counting	Enables counting
3	1) Disables counting 2) Sets output immediately high	Initiates counting	Enables counting
4	Disables counting	—	Enables counting
5	—	Initiates counting	—

3-7. ADDRESSING

As listed in Table 3-3, the PIT uses four I/O addresses. Addresses 00D0, 00D2, and 00D4, respectively, are used in loading and reading the count in counter 0, 1, and 2. Address 00D6 is used in writing the mode control word to the desired counter.

3-8. INITIALIZATION

To initialize the PIT chip, perform the following:

a. Write a mode control word for counter 0 to 00D6. Note that all mode control words are written to 00D6, since the mode control word must specify which counter is being programmed. (Refer to Figure 3-1.)

   Table 3-5 provides a sample subroutine for writing mode control words to all three counters.

b. Assuming the mode control word has selected a 2-byte load, load least-significant byte of count into counter 0 at 00D0. (Count value to be loaded is described in paragraph 3-14.) Table 3-6 provides a sample subroutine for loading 2-byte count value.

c. Load most-significant byte of count into counter 0 at 00D0.

NOTE

Be sure to enter the downcount in two bytes if the counter was programmed for a two-byte entry in the mode control word. Similarly enter the downcount value in BCD if the counter was so programmed.

d. Repeat steps b and c for counters 1 and 2.

3-9. OPERATION

The following paragraphs describe operating procedures for a counter read, clock frequency divide/ratio selection, and interrupt timer counter selection.

3-10. COUNTER READ

There are two methods that can be used to read the contents of a particular counter. The first method involves a simple read of the desired counter. The only requirements with this method is that, in order to ensure stable count reading, the desired counter must be inhibited by controlling its gate input.

The second method allows the counter to be read on-the-fly. The recommended procedure is to use a mode control word to latch the contents of the count register. This ensures that the count reading is accurate and stable. The latched value of the count can then be read.

NOTE

If a counter is read on the fly, it is mandatory to complete the read procedure. That is, if two bytes were programmed to the counter, then two bytes must be read before any other operations are performed with that counter.

To read the count of a particular counter, proceed as follows (a typical counter read subroutine is given in Table 3-7):

a. Write counter register latch control word (Figure 3-3) to port 00D6. The control word specifies the desired counter and selects the counter latching operation.

b. Perform a read operation of the desired counter. (Refer to Table 3-3 for counter addresses.)

NOTE

Be sure to read one or two bytes, whichever was specified in the initialization mode control word. For two bytes. read in the order specified.

Table 3-5. Typical PIT Control Word Subroutine

```
;INTTMR INITIALIZES COUNTERS 0,1,2.
;COUNTERS 0 AND 1 ARE INITIALIZED AS INTERRUPT TIMERS.
;COUNTER 2 IS INITIALIZED AS PROGRAMMABLE ONE-SHOT.
;ALL THREE COUNTERS ARE SET UP FOR 16-BIT OPERATION.
;DESTROYS-AL.

            PUBLIC    INTTMR

INTTMR:     MOV       AL,30H          ;MODE CONTROL WORD FOR COUNTER 0
            OUT       0D6H,AL
            MOV       AL,70H          ;MODE CONTROL WORD FOR COUNTER 1
            OUT       0D6H,AL
            MOV       AL,B2H          ;MODE CONTROL WORD FOR COUNTER 2
            OUT       0D6H,AL
            RET

            END
```

Table 3-6. Typical PIT Counter Value Load Subroutine

```
;LOAD0 LOADS COUNTER 0 FROM CX, CH IS MSB, CL IS LSB.
;USES-D,E: DESTROYS—AL.

            PUBLIC    LOAD0

LOAD0:      MOV       AL,CL           ;GET LSB
            OUT       0D0H,AL
            MOV       AL,CH           ;GET MSB
            OUT       0D0H,AL
            RET

            END
```

Table 3-7. Typical PIT Counter Read Subroutine

```
;READ1 READS COUNTER 1 ON-THE-FLY INTO CX. MSB IN CH, LSB IN CL.
;DESTROYS-AL,CX.

            PUBLIC    READ1

READ1:      MOV       AL,40H          ;MODE WORD FOR LATCHING COUNTER 1 VALUE
            OUT       0D6H,AL
            IN        AL,0D2H         :LSB OF COUNTER
            MOV       CL,AL
            IN        AL,0D2H         ;MSB OF COUNTER
            MOV       CH,AL
            RET

            END
```

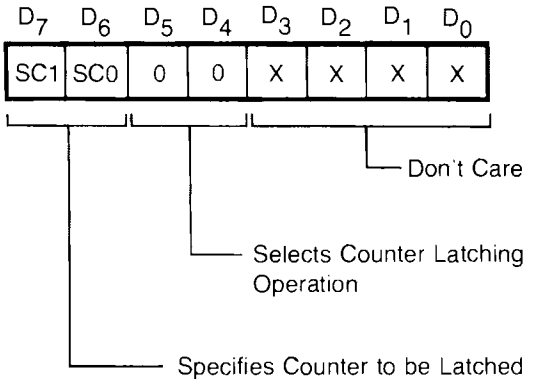


Figure 3-3. PIT Counter Register Latch Control Word Format

3-11. CLOCK FREQUENCY/DIVIDE RATIO SELECTION

The default timer input frequency to counters 0 and 2 is 1.228 MHz. Counter 1 is 153.6 KHz. The timer input frequency is divided by the counters to generate TIMER 0 INTR and TIMER 1 INTR.

Each counter must be programmed with a count value N. When count value N is loaded into a counter, it becomes the clock divisor. To derive the output frequency (modes 2, 3) or time interval (modes 1, 4, 5) for any given count, use the following formula:

$$\text{Output frequency} = \frac{F}{N}$$

$$\text{Time interval} = \frac{N}{F}$$

Where N = count value
F = 1.2288 MHz, the timer clock frequency

3-12. RATE GENERATOR/INTERVAL TIMER

Table 3-8 shows the maximum and minimum rate generator frequencies and timer intervals for the counters. The table also provides the maximum and minimum generator frequencies and time intervals that may be obtained by connecting two counters in series.

3-13. INTERRUPT TIMER

To program an interval timer for an interrupt on terminal count, program the appropriate timer for the correct operating mode (mode 0) in the control word. Then load the count value (N), which is derived by:

N = TF
Where:
N = count value for counter.
T = desired interrupt time interval in seconds.
F = input clock frequency.

Table 3-8. PIT Rate Generator Frequencies and Timer Intervals

	Single Timer[1] (Counter 0)		Single Timer[2] (Counter 1)		Dual Timer[3] (0 and 1 in Series)	
	Minimum	Maximum	Minimum	Maximum	Minimum	Maximum
Rate Generator (frequency)	18.75 Hz	614.4 kHz	2.344 Hz	76.8 kHz	0.00029 Hz	307.2 kHz
Real-Time Interrupt (interval)	1.63 μsec	53.3 msec	13 μsec	426.67 msec	3.26 μsec	58.25 minutes

NOTES:
1. Assuming a 1.23-MHz clock input.
2. Assuming a 153.6-kHz clock input.
3. Assuming Counter 0 has 1.23-MHz clock input.

Table 3-9 shows the count value (N) required for several time intervals (T) that can be generated for the counters.

Table 3-9. PIT Time Intervals Vs. Timer Counts

T	N*
10 μsec	12
100 μsec	123
1 msec	1229
10 msec	12288
50 msec	61440

*Count Values (N) assume clock is 1.23 MHz. Count Values (N) are in decimal.

3-14. 8251A PCI PROGRAMMING

The PCI converts parallel output data into virtually any series output data format (including IBM BiSync) for half- or full-duplex operation. The PCI also converts serial input data into parallel data format.

Prior to transmitting or receiving data, the PCI must be loaded with a set of control words. These control words, which define the complete functional operation of the PCI, must immediately follow a reset (internal or external). The control words are either a Mode instruction or a Command instruction.

3-15. MODE INSTRUCTION FORMAT

The Mode instruction word defines the general characteristics of the PCI and must follow a reset operation. Once the Mode instruction word has been written into the PCI, sync characters or command instructions may be inserted. The Mode instruction word defines the following:

a. For Sync Mode:
   (1) Character length
   (2) Parity enable
   (3) Even/odd parity generation and check
   (4) External sync detect
   (5) Single or double character synch

b. For Async Mode:
   (1) Baud rate factor (X16-X64)
   (2) Character length
   (3) Parity enable
   (4) Even/odd parity generator and check
   (5) Number of stop bits

Instruction word and data transmission formats for synchronous and asynchronous modes are shown in Figures 3-4 through 3-8.

3-16. SYNC CHARACTERS

Sync characters are written to the PCI in the synchronous mode only. The PCI can be programmed for either one or two sync characters; the format of the sync character is at the option of the programmer.

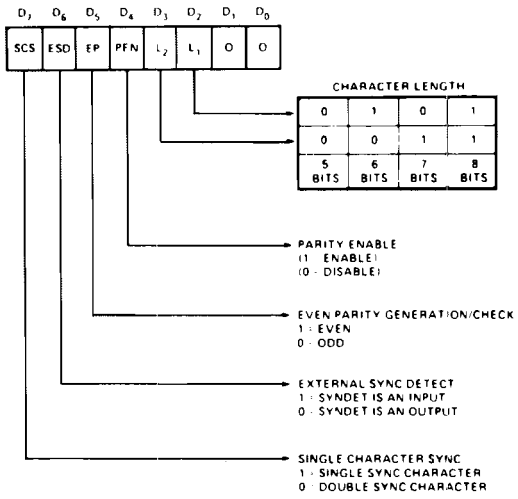


Figure 3-4. PCI Synchronous Mode Instruction Word Format

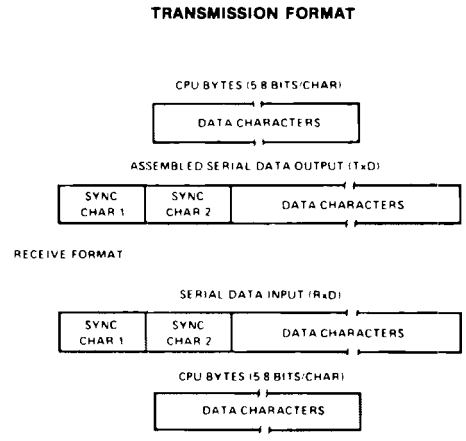


Figure 3-5. PCI Synchronous Mode Data Format

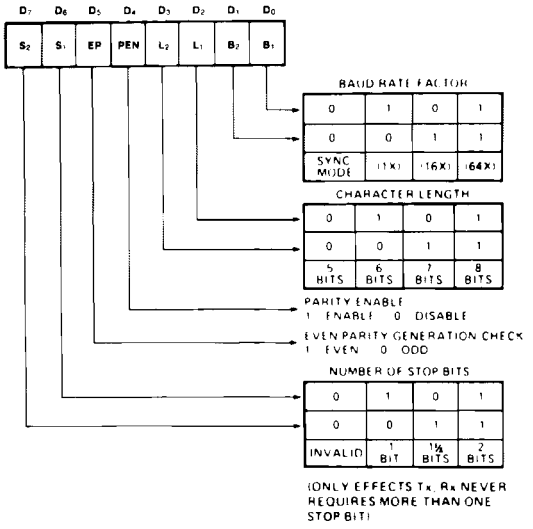


Figure 3-6. PCI Asynchronous Mode Instruction Word Format

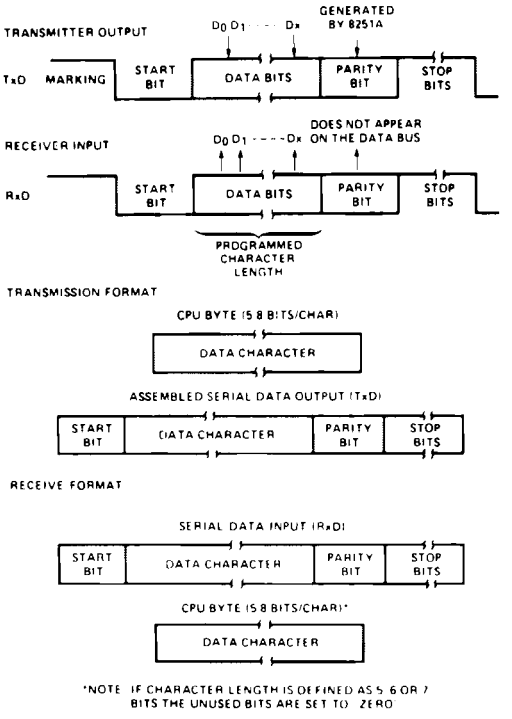


Figure 3-7. PCI Asynchronous Mode Data Format

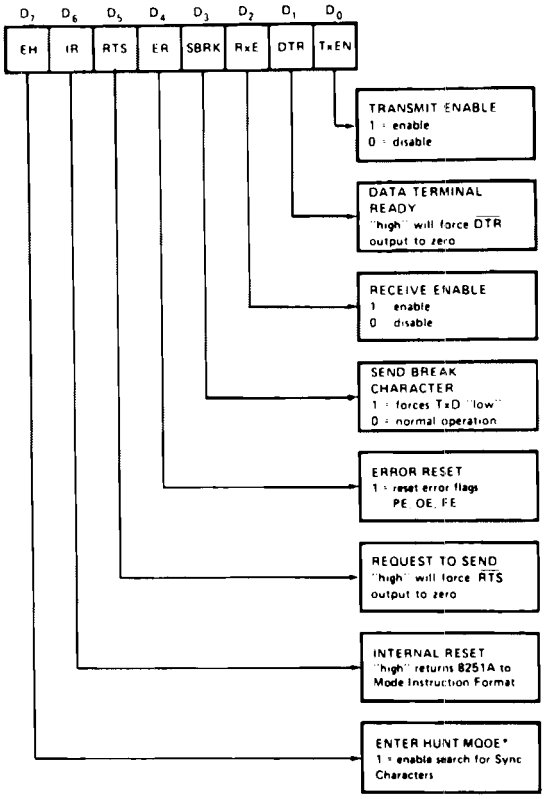


Figure 3-8. PCI Command Instruction Word Format

3-17. COMMAND INSTRUCTION FORMAT

The Command instruction word shown in Figure 3-8 controls the operation of the addressed PCI. A Command instruction must follow the mode and/or sync words and, once the Command instruction is written, data can be transmitted or received by the PCI.

It is not necessary for a Command instruction to precede all data transactions; only those transactions that require a change in the Command instruction. An example is a change in the enable transmit bit or enable receive bit. Command instructions can be written to the PCI at any time after the mode instruction.

After initialization, always read the PCI status and check for the TxRDY bit prior to writing either data or command words to the PCI. This ensures that any prior input is not overwritten and lost. Note that issuing a Command instruction with bit 6 (IR) set will return the PCI to the Mode instruction format.

3-18. RESET

To change the Mode instruction word, the PCI must receive a Reset command. This can be either a hardware reset or a reset generated by bit 6 of the Command Instruction. The next word written to the PCI after a Reset command is assumed to be a Mode instruction. Similarly, for sync mode, the next word after a Mode instruction is assumed to be one or more sync characters. All control words written into the PCI after the Mode instruction (and/or the sync character) are assumed to be Command instructions.

3-19. ADDRESSING

The PCI device uses two consecutive pairs of addresses. The lower of the two addresses in each pair is used to read and write I/O data; the upper address in each pair is used to write mode and command words and to read the PCI status. (Refer to Table 3-10).

Table 3-10. PCI Address Assignments

I/O Address (hexadecimal)	Command	Function	Direction
DA or DE	OUTPUT	CONTROL	CPU → PCI
D8 or DC	OUTPUT	DATA	CPU → PCI
DA or DE	INPUT	STATUS	PCI → CPU
D8 or DC	INPUT	DATA	PCI → CPU

3-20. INITIALIZATION

A typical PCI initialization and I/O data sequence is presented in Figure 3-9. The PCI device is initialized in four steps:

a. Reset PCI to Mode instruction format.

b. Write four sets of zeros to the PCI. This will prevent spurious operation.

c. Write Mode instruction word. One function of mode word is to specify synchronous or asynchronous operation.

d. If synchronous mode is selected write one or two sync characters as required.

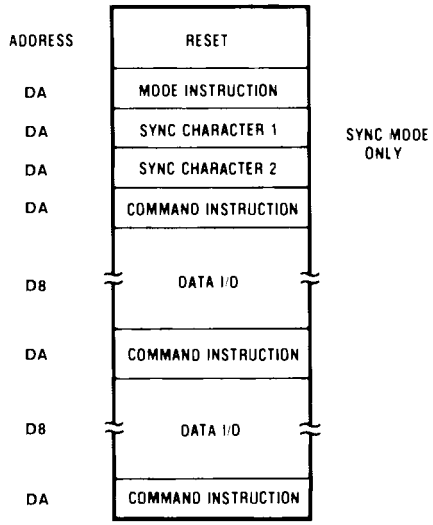
e. Write Command instruction word.

To avoid spurious interrupts during PCI initialization, disable the PCI interrupt. This can be done by either masking the appropriate interrupt request input at the 8259A PIC or by disabling the 8088 microprocessor interrupts by executing a CLI instruction.

First, reset the PCI device by writing a Command instruction to Port 00DA (or 00DE). The Command instruction must have bit 6 set (IR = 1); all other bits are immaterial.

NOTE

This reset procedures should be used only if the PCI has been completely initialized, or the initialization procedure has reached the point where the PCI is ready to receive a Command word. For example, if the reset command is written when the initialization sequence calls for a sync character, then subsequent programming will be in error.



*The second sync character is skipped if Mode instruction has programmed PCI to single character internal sync mode. Both sync characters are skipped if Mode instruction has programmed PCI to async mode.

Figure 3-9. Typical PCI Initialization and Data I/O Sequence

Next write a Mode instruction word to the PCI. (See Figure 3-4 through 3-7.) A typical subroutine for writing both Mode and Command instructions is given in Table 3-11.

If the PCI is programmed for the synchronous mode, write one or two sync characters depending on the transmission format.

Finally, write a Command instruction word to the PCI. Refer to Figure 3-8 and Table 3-11.

IMPORTANT: During initialization, the 8251A PCI requires a minimum recovery time of 6.5 microseconds (16 PCI clock cycles) between back-to-back writes in order to set up its internal registers. This recovery time can be satisfied by the CPU performing several dummy instructions between back-to-back writes to the 8251A to create a minimum delay

of 6.5 microseconds. The following example will create a delay of approximately 8 microseconds.

```
        MOV     AL,04EH     ;PCI MODE WORD
        OUT     0DAH,AL     ;FIRST PCI WRITE
        MOV     CX,1        ;DELAY
TAG:    LOOP    TAG         ;DELAY
        MOV     AL,037H     ;PCI COMMAND WORD
        OUT     0DAH,AL     ;SECOND PCI WRITE
```

This precaution applies only to the PCI initialization and does not apply otherwise.

Table 3-12 shows a typical PCI Data Character Read Subroutine. Table 3-13 shows a typical PCI Data Character Write Subroutine.

Table 3-11. Typical PCI Mode or Command Instruction Subroutine

```
;CMD2 OUTPUTS CONTROL WORD TO USART FROM AL REGISTER.
;USES-AL, STAT0; DESTROYS-NOTHING.
;CALLING ROUTINE PASSES CONTROL WORD TO AL BEFORE CALLING CMD2.

            PUBLIC    CMD2
            EXTRN     STAT0

CMD2:       PUSH      AX
            PUSH      F
LP:         CALL      STAT0
            AND       AL,1              ;CHECK TXRDY
            JZ        LP                ;TXRDY MUST BE TRUE
            POPF
            POP       AX
51INT:      OUT       0DAH,AL           ;ENTER HERE FOR INITIALIZATION
            RET

            END
```

Table 3-12. Typical PCI Data Character Read Subroutine

```
;RX1 READS DATA CHARACTER FROM USART AND RETURNS DATA IN AL REGISTER.
;USES-STAT0; DESTROYS-AL, FLAGS.

            PUBLIC    RX1
            EXTRN     STAT0

RX1:        CALL      STAT0
            AND       AL,2              ;CHECK FOR RXRDY TRUE
            JZ        RX1
RXA1:       IN        AL,0D8H           ;ENTER HERE IF RXRDY IS TRUE
            RET

            END
```

Table 3-13. Typical PCI Data Character Write Subroutine

```
;TX1 WRITES DATA CHARACTER FROM REG AL TO USART.
;USES-AL, STAT0; DESTROYS-FLAGS.
;CALLING ROUTINE PUTS DATA INTO AL BEFORE CALLING TX1.

            PUBLIC    TX1
            EXTRN     STAT0

TX1:        PUSH      AX
TX11:       CALL      STAT0
            AND       AL,1              ;CHECK FOR TXRDY TRUE
            JZ        TX11
            POP       AX
TXA1:       OUT       0D8H,AL           ;ENTER HERE IF TXRDY IS TRUE
            RET

            END
```

The TxRDY and RxRDY outputs of the PCI are available at the priority interrupt jumper matrix. If, for instance, TxRDY and RxRDY are input to the 8259A PIC, the PIC resolves the priority and interrupts the CPU, TxRDY and RxRDY are also available in the status word.

Status Read. The CPU can determine the status of a serial I/O port by issuing an I/O Read Command to the upper port (00DA or 00DE) of the PCI. The format of the status word is shown in Figure 3-10. A typical status read subroutine is given in Table 3-14.

3-21. 8255A PPI PROGRAMMING

The iSBC 88/25 board has a total of 24 parallel I/O lines, grouped into three ports: C8, CA, and CC. All lines exit the board via connector J1. One 8255A PPI device is used to control all three ports. Line identification is provided in Table 2-26.

Each of the three parallel I/O ports may be programmed independently. However, as implemented on the iSBC 88/25 board, some lines have restricted use in certain modes. The modes allowed on the iSBC

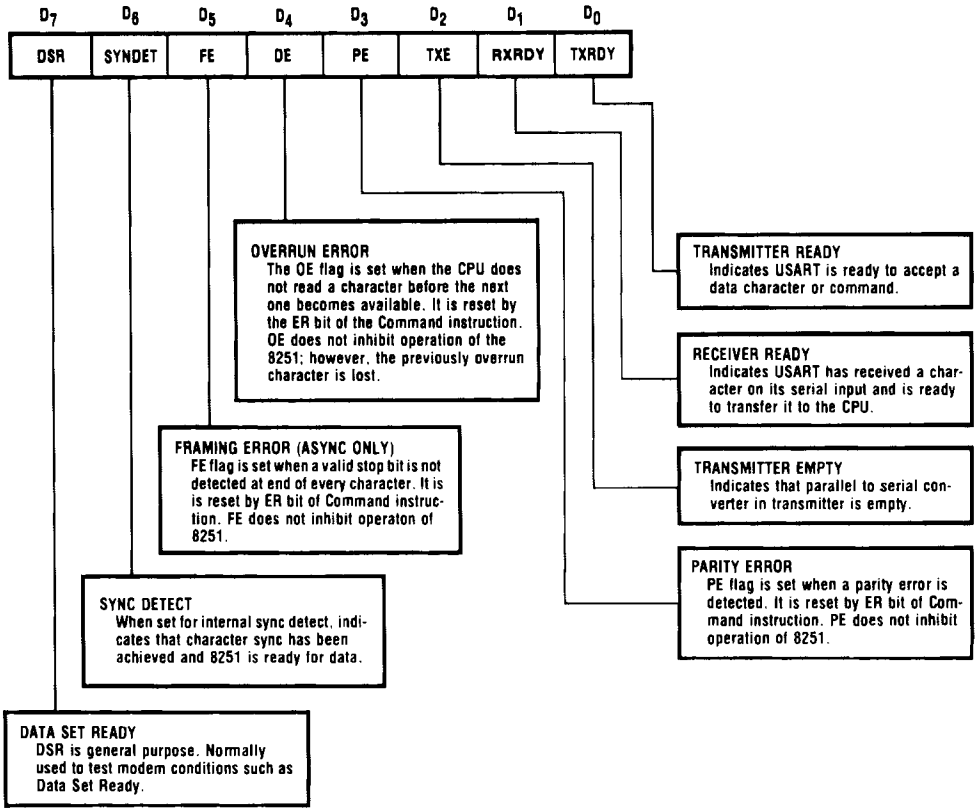


Figure 3-10. PCI Status Read Format

Table 3-14. Typical PCI Status Read Subroutine

```
;STAT0 READS STATUS FROM USART.
;DESTROYS-AL.

            PUBLIC    STAT0

STAT0:      IN        AL,0DEH          ;GET STATUS
            RET

            END
```

88/25 board are listed in Table 3-15. Notice that each half of port CC may be programmed independently. These configurations are shown in Table 3-24, along with configurations for ports C8 and CA.

Default jumpers set the port C8 transceivers to the output (transmit) mode. Optional jumper connections allow the bus transceivers to be set to either the input mode or a bit-programmable input/output mode. Refer to Tables 2-10, 2-11, and 2-12 for complete jumper information.

Ports CA and CC do not have bus transceivers installed at the factory. Line drivers or terminators can be installed for these ports as described in Section 2-12.

In order to use any of the parallel port lines, the 8255A PPI device must first be initialized and programmed for the desired mode and direction of data flow. Sections 3-23 through 3-26 provide this information.

3-22. CONTROL WORD FORMAT

The control word format shown in Figure 3-11 is used to initialize the PPI port. Group A (control word bits 3 through 6) defines the operating mode for port A and the upper four bits of port C. Group B (control word bits 9 through 2) defines the operating mode for port B and the lower four bits of port C. (Refer to Table 3-16 for port identification). Bit 7 of the control word controls the mode set flag. Control words are sent to port CE (Table 3-16). There are restrictions associated with the use of certain ports in modes 1 and 2. Refer to Table 2-12 for restrictions.

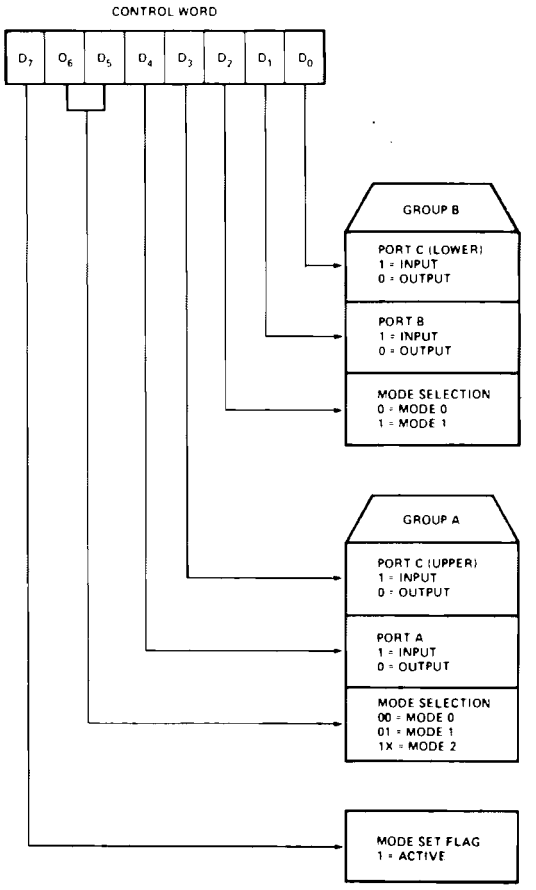


Figure 3-11. PPI Control Word Format

Table 3-15. Parallel Port Configurations

Port C8
Mode 0, input
Mode 0, output (latched)
Mode 1, input (strobed)
Mode 1, output (latched)
Mode 2, bidirectional
Port CA
Mode 0, input
Mode 0, output (latched)
Mode 1, input (strobed)
Mode 1, ouput (latched)
Port CC *
Mode 0, 8-bit input
Mode 0, 8-bit output (latched)
Mode 0, split (4-bit input, 4-bit output)
*Control mode may depend on mode of other ports; see table 2-10.

3-23. ADDRESSING

The PPI uses four consecutive even addresses (00C8 through 00CE) for data transfer, obtaining the status of Port C (00CC), and for port control. (Refer to Table 3-16.)

Table 3-16. Parallel Port I/O Address

8255A Device Port	Eight-Bit Address (hexadecimal)
8255A Port (A)	C8
8255A Port (B)	CA
8255A Port (C)	CC
8255A Control	CE For I/O write only

3-24. INITIALIZATION

To initialize the PPI, write a control word to port 00CE. Refer to Figure 3-11 and Table 3-17 and assume that the control word is 92 (hexadecimal).The example in Table 3-17 initializes the PPI as follows:

a. Mode Set Flag active
b. Port A (00C8) set to Mode 0 Input
c. Port C (00CC) upper set to Mode 0 Output
d. Port B (00CA) set to Mode 0 Input.
e. Port C (00CC) lower set to Mode 0, Output.

After RESET each port of the PPI is initialized to Mode 0, Input.

3-25. OPERATION

The primary considerations in determining how to operate each of th three I/O ports are:

a. Choice of operating mode (as defined in Table 3-15);
b. Direction of data flow (input, output or bidirectional), (see Table 3-20); and
c. Choice of driver/terminator networks.

After the PPI has been initialized, the operation is completed by simply performing a read or write to the appropriate port.

A typical read subroutine for Port A is given in Table 3-18. A typical write subroutine for Port C is given in Table 3-19.

Table 3-17. Typical PPI Initialization Subroutine

```
;INTPAR INITIALIZES PARALLEL PORT MODES.
;DESTROYS-AL.

            PUBLIC    INTPAR

INTPAR:     MOV       AL,92H          ;MODE WORD TO PPI PORT A&B IN,C OUT
            OUT       0CEH, AL
            RET

            END
```

Table 3-18. Typical PPI Port Read Subroutine

```
;AREAD READS A BYTE FROM PORT A INTO REG AL.
;DESTROYS-AL.

            AREAD

AREAD:      IN        AL,0C8H         ;GET BYTE
            RET

            END
```

Table 3-19. Typical PPI Port Write Subroutine

```
;COUT OUTPUTS A BYTE FROM REG AL TO PORT C.
;USES-AL; DESTROYS-NOTHING.
;THE CALLING ROUTINE PASSES THE DATA BYTE TO AL BEFORE CALLING COUT.
            PUBLIC    COUT

COUT:       OUT       0CCH,AL         ;OUTPUT BYTE
            RET

            END
```

Single Bit Set/Reset Feature

Any of the eight bits of Port C (board port CC) can be Set or Reset using a single output instruction (see Figure 3-12). This feature reduces software requirements in Control-based applications.

When Port C is being used as status/control for Port A or B, Port C I/O bits and INTE bits can be set or reset by using the Bit Set/Reset operation. The IBF, OBF and INTR outputs will not be modified by either a write to Port C or a bit set/reset command.

Mode Combinations

Table 3-20 summarizes the various mode combinations possible with ports A and B of the PPI, and indicates how each port C bit can be used. This table can serve as a useful starting point for selecting your particular configuration. Once you select the desired mode combination and the port C bit assignments are made, refer to the jumper configuration table (2-12) for implementation details.

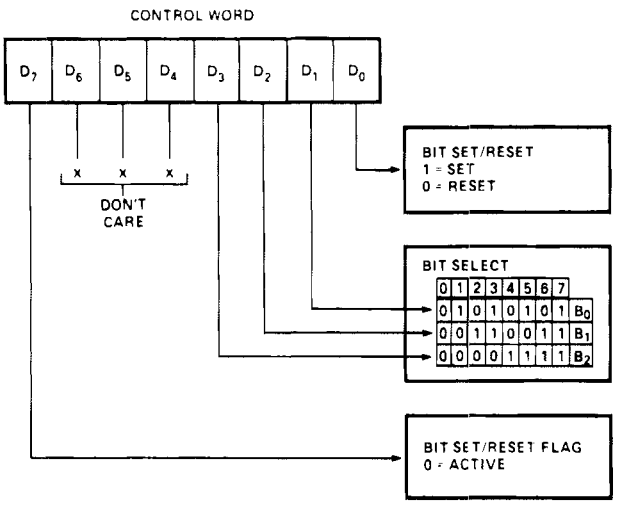


Figure 3-12. PPI Port C Bit Set/Reset Control Word Format

Table 3-20. Parallel I/O Interface Configurations

Configuration Number	PPI Port A (C8)	PPI Port B (CA)	PPI Port C (CC) Lower				PPI Port C (CC) Upper			
			C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7
1	MODE 0-IN	MODE 0-I/O	— I/O —				— I/O —			
2	MODE 0-OUT	MODE 0-I/O	— I/O —				— I/O —			
3	MODE 0-IN	MODE 1-I/O	R	R	R	I	O	O	O	U
4	MODE 0-IN	MODE 1-I/O	R	R	R	O	I	I	I	U
5	MODE 0-OUT	MODE 1-I/O	R	R	R	I	O	O	O	U
6	MODE 0-OUT	MODE 1-I/O	R	R	R	O	I	I	I	U
7	MODE 1-IN	MODE 0-I/O	I	I	I	R	R	R	O	O
8	MODE 1-IN	MODE 0-I/O	O	O	O	R	R	R	I	I
9	MODE 1-OUT	MODE 0-I/O	I	I	I	R	O	O	R	R
10	MODE 1-OUT	MODE 0-I/O	O	O	O	R	I	I	R	R
11	MODE 1-IN	MODE 1-I/O	R	R	R	R	R	R	I	I
12	MODE 1-IN	MODE 1-I/O	R	R	R	R	R	R	O	O
13	MODE 1-OUT	MODE 1-I/O	R	R	R	R	I	I	R	R
14	MODE 1-OUT	MODE 1-I/O	R	R	R	R	O	O	R	R
15	MODE 2-B	MODE 0-I/O	U	I	I	R	R	R	R	R
16	MODE 2-B	MODE 0-I/O	U	O	O	R	R	R	R	R
17	MODE 2-B	MODE 1-I/O	R	R	R	R	R	R	R	R

NOTES:

I - INPUT
O - OUTPUT
I/O - INPUT OR OUTPUT
B - BIDIRECTIONAL

R - Reserved for status control of ports A or B

U - No unused drivers/terminators available. These bits may be used, however, to connect to the serial I/O interface or the Interval Timer.

3-26. 8259A PIC PROGRAMMING

The 8259A PIC functions as an overall manager in an interrupt-driven system environment. It accepts requests from the peripheral equipment, determines which of the incoming requests is of the highest importance (priority), ascertains whether the incoming request has a higher priority value than the level currently being serviced, and may issue an interrupt to the CPU based on this determination.

The on-board master 8259A PIC handles up to eight vectored priority interrupts and has the capability of expanding the number of priority interrupts by cascading one or more of its interrupt input lines with slave 8259A PIC's. (Refer to paragraph 2-14.)

The basic functions of the PIC are to (1) resolve the priority of interrupt requests, (2) issue a single interrupt request to the CPU based on that priority, and (3) send the CPU an interrupt type number for servicing the interrupting device.

3-27. INTERRUPT PRIORITY MODES

The PIC can be programmed to operate in one or more of the following modes:

a. Fully Nested Mode
b. Special Fully Nested Mode
c. Automatic Rotating Mode
d. Specific Rotating Mode
e. Special Mask Mode
f. Poll Mode

3-28. FULLY NESTED MODE. In this mode, the PIC input signals are assigned a priority from 0 through 7. The PIC operates in this mode unless specifically programmed otherwise. Interrupt IR0 has the highest priority and IR7 has the lowest priority. When an interrupt is acknowledged, the highest priority request is available to the CPU. Lower priority interrupts are inhibited; higher priority interrupts will be able to generate an interrupt that will be acknowledged if the CPU has enabled its own interrupt through software. The End-Of-Interrupt (EOI) command from the CPU is required to reset the PIC for the next interrupt.

3-29. SPECIAL FULLY NESTED MODE. This mode is used only when one or more PIC's are slaved to the master PIC, in which case the priority is conserved within the slave PIC's.

The operation in the special fully nested mode is the same as the fully nested mode except as follows:

a. When an interrupt from slave PIC is being serviced, that particular PIC is not locked out from the master PIC priority logic. That is, further interrupts of higher priority within this slave PIC will be recognized and the master PIC will initiate an interrupt to the CPU.
b. When exiting the interrupt service routine, the software must check to determine if another interrupt is pending from the same slave PIC. This is done by sending an End-Of-Interrupt (EOI) command to the slave PIC and then reading its In-Service (IS) register. If the IS register is clear (empty), an EOI command is sent to the master PIC. If the IS register is not clear (interrupt pending), no EOI command should be sent to the master PIC.

3-30. AUTOMATIC ROTATING MODE. In this mode, the interrupt priority rotates. Once an interrupt on a given input is serviced, that interrupt assumes the lowest priority. Thus, if there are a number of simultaneous interrupts, the priority will rotate among the interrupts in numerical order. For example, if interrupts IR4 and IR6 request service simultaneously, IR4 will receive the highest priority. After service, the priority level rotates so that IR4 has the lowest priority and IR5 assumes the highest priority. In the worst case, seven other interrupts are serviced before IR4 again has the highest priority. Of course, if IR4 is the only request, it is serviced promptly. The priority shifts when the PIC receives an End-Of-Interrupt (EOI) command.

3-31. SPECIFIC ROTATING MODE. In this mode, the software can change interrupt priority by specifying the bottom priority, which automatically sets the highest priority. For example, if IR5 is assigned the bottom priority, IR6 assumes the highest priority. In specific rotating mode, the priority can be rotated by writing a Specific Rotate at EOI (SEOI) command to the PIC. This command contains the binary code of the interrupt being serviced; that interrupt is reset as the bottom priority. In addition, the bottom priority interrupt can be fixed at any time by writing a set priority command to the IC.

3-32. SECIAL MASK MODE. In the fully nested mode all IR levels of priority equal to or below the interrupt in service are inhibited. To enable lower priority interrupts in this situation, the Special Mask Mode must be used.

Working on conjunction with the IMR, the special mask mode enables interrupts from all levels *except* the level in service. This is done by masking the level that is in service and any other unwanted interrupt levels with OCW1 and then issuing the special mask mode command. To terminate the special mask mode, OCW3 is written with ESMM = 1 and SMM = 0.

3-33. POLL MODE. In this mode the CPU internal Interrupt Enable flip-flop is clear (interrupts disabled) and a software subroutine is used to initiate a Poll command. In the Poll Mode, the addressed PIC treats an I/O Read Command as an interrupt acknowledge, sets its In-Service flip-flop if there is a pending interrupt request, and reads the priority level. This mode is useful if there is a common service routine for several devices.

3-34. STATUS READ

Interrupt request inputs are handled by the following three internal PIC registers:

a. Interrupt Request Register (IRR), which stores all interrupt levels that are requesting service.

b. In-Service Register (ISR), which stores all interrupt levels that are being serviced.

c. Interrupt Mask Register (IMR), which stores the interrupt request lines which are masked.

These registers can be read by writing a suitable OCW3 command word and then performing a read operation. No OCW3 is required for reading the IMR. There is no need to write an OCW3 before each identical status read operation.

3-35. INITIALIZATION COMMAND WORDS

The on-board master PIC and each slave PIC requires a separate initialization sequence to work in a particular mode. The initialization sequencee requires three Initialization Command Words (ICW's) for a single PIC system and requries four ICW's for a master PIC with one to eight slaves. The ICW formats are shown in Figure 3-13.

~~The first Initialization Command Word (ICW1), which is required in all modes of operation, consists of the following:~~

a. Bits 0 and 4 are both 1's and identify the word as ICW1 for an 8088 CPU operation.

b. Bit 1 denotes whether or not the PIC is employed in a multiple PIC configuration. For a single master PIC configuration (no slaves), bit 1=1; for a master with one or more slaves, bit 1=0.

NOTE

Bit 1=0 when programming a slave PIC.

c. Bit 3 establishes whether the interrupts are requested by a positive true level input or requested by a low-to-high input. This applies to all input requests handled by the PIC. In other words, if bit 3=0, a low-to-high transition is required to request an interrupt on any of the eight levels handled by the PIC.

The second Initialization Command Word (ICW2) represents the interrupt type (identifier) and is required by the 8088 CPU during interrupt processing. The 8088 CPU can handle 256 different interrupt types. ICW2 consists of the following:

a. Bits D3-D7 (T3-T7) represent the five most significant bits of the interrupt type. These are supplied by the programmer.

b. Bits D0-D2 represent the interrupt level requesting service. These bits are provided by the 8259A during interrupt processing and make up the lower significant bits of interrupt type. These bits should be programmed as 0's when initializing the PIC.

NOTE

The 8088 CPU multiples the vector byte by four. This value is then used by the CPU as the vector address.

Table 3-21 lists the interrupt type pointer contents for interrupts IR0-IR7.

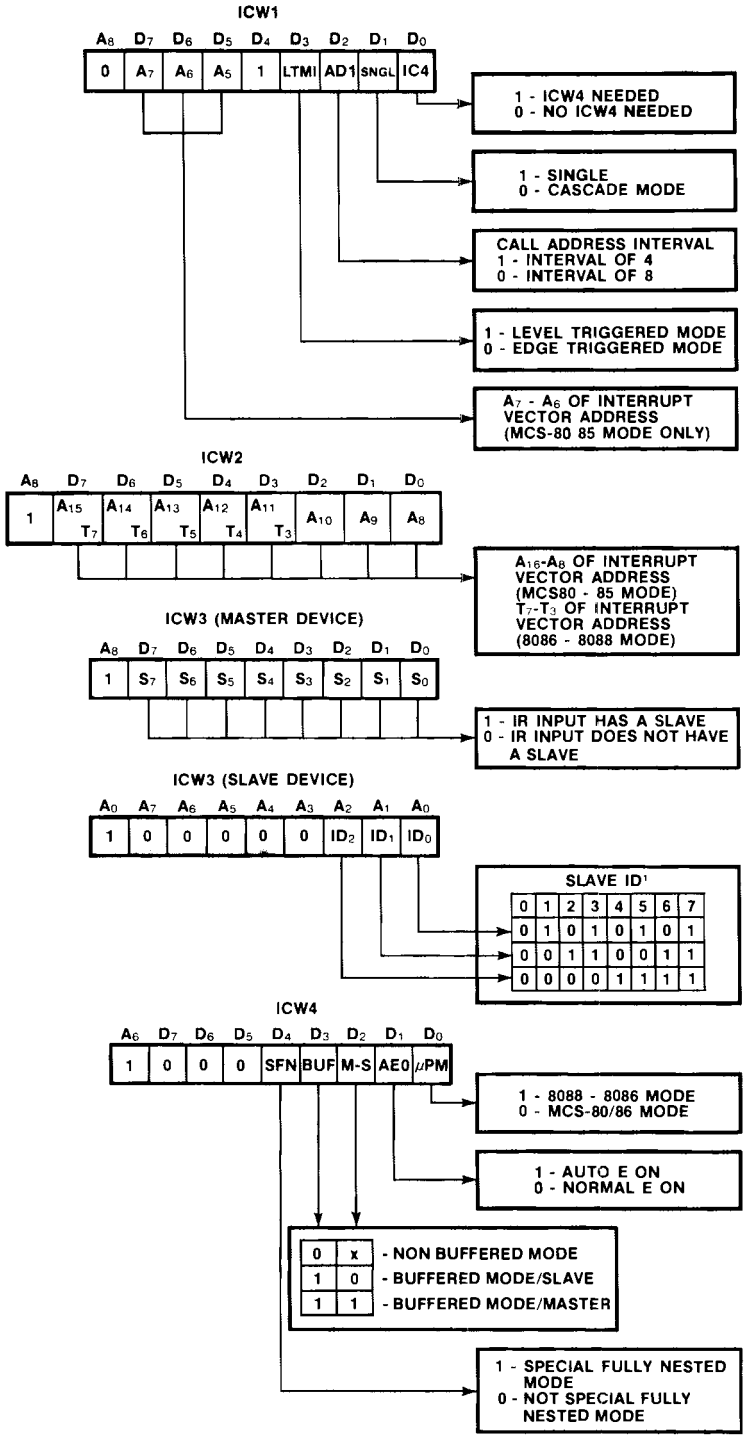
~~Table 3-21. Interrupt Type Pointers~~

~~Contents of Interrupt Vector Byte for iSBC 88/25 System~~

	D7	D6	D5	D4	D3	D2	D1	D0
IR7	T7	T6	T5	T4	T3	1	1	1
IR6	T7	T6	T5	T4	T3	1	1	0
IR5	T7	T6	T5	T4	T3	1	0	1
IR4	T7	T6	T5	T4	T3	1	0	0
IR3	R7	R6	R5	R4	R3	0	1	1
IR2	T7	T6	T5	T4	T3	0	1	0
IR1	T7	T6	T5	T4	T3	0	0	1
IR0	T7	T6	T5	T4	T3	0	0	0

The third Initialization Command Word (ICW3) is required only if bit 1=0 in ICW1, specifying that multiple PIC's are used; i.e., one or more PIC's are slaved to the on-board master PIC. ICW3 programming can be in one of two formats: master mode format and slave mode format.

a. For master mode, the D0-D7 (S0-S7) bits correspond to the IR0-IR7 bits of the master PIC. For example, if a slave PIC is connected to the master PIC IR3 input, code bit 3=.



NOTE 1: SLAVE IO IS EQUAL TO THE CORRESPONDING MASTER R INPUT.

Figure 3-13. PIC Initialization Command Word Formats

b. For a slave PIC, the D0-D2 (ID0-ID2) bits identify the master IR line that the slave PIC is connected to during an interrupt cycle. The slave compares its cascade input (generated by the master PIC0 with these bits and, if they are equal, the slave releases an interrupt type pointer upon the reception of the second INTA during interrupt processing. For example, if a slave is connected to the master interrupt line IR5, code bits ID0-ID2=101.

The fourth Initialization Command Word (ICW4), which is required for all modes of operation, consists of the following:

a. Bit D0 is a 1 to identify that the word is for an 8088 CPU.

b. Bit D1 (AEO1) programs the end-of-interrupt function. Code bit 1=1 if an EOI is to be automatically executed (hardware). Code bit 1=0 if an EOI command is to be generated by software before returning from the service routine.

c. Bit D2 (M/S) specifies if ICW4 is addressed to a master PIC or a slave PIC. For example, code bit 2=1 in ICW4 for the master PIC. ~~If bit D3 (BUF) is zero, bit D2 has no function~~.

d. Bit D3 (BUF) specifies whether the 8259A is operation in the buffered or nonbuffered mode. For example, code bit 3=1 for buffered mode.

NOTE

~~The master PIC in an iSBC 88/25, with or without slaves, must be operated in the buffered mode.~~

e. Bit D4 (SFNM) programs the fully nested or special fully nested mode. (Refer to paragraph 3-29 and 3-30).

In summary, three or four ICW's are required to initialize the master and each slave PIC. Specifically

- Master PIC — No Slaves
  - ICW1
  - ICW2
  - ICW3/4
- Master PIC — With Slave(s)
  - ICW1
  - ICW2
  - ICW3
  - ICW4
- Each Slave PIC
  - ICW1
  - ICW2
  - ICW3
  - ICW4

3-36. OPERATION COMMAND WORDS

After being initialized, the master and slave PIC's can be programmed at any time for various operating modes. The Operation Command Word (OCW) formats are shown in Figure 3-14.

3-37. ADDRESSING

The master PIC uses Port 00C0 or 00C2 to write initialization and operation command words and Port 00C4 or 00C6 to read status, poll, and mask bytes. Addresses for the specific functions are provided in Table 3-3.

Slave PIC's, if employed, are accessed via the Multibus interface and their addresses are determined by the hardware designer.

3-38. INITIALIZATION

Table 3-22 provides a typical PIC initialization subroutine for a PIC operated in the non-bus vectored mode; Table 3-23 and 3-24 are typical master PIC and slave PIC initialization subroutines for the bus vectored mode. To initialize the PIC's (master and slaves), proceed as follows:

a. Disable system interrupts by executing a CLI (Clear Interrupt Flag) instruction.

b. Initialize master PIC by writing ICW's in the following sequence:
   (1) Write ICW1 to Port 00C0 and ICW2 to Port 00C2.
   (2) If slave PIC's are used, write ICW3 and ICW4 to Port 00C2. If no slave PIC's are used, omit ICW3 and write ICW4 only to Port 00C2.

c. Initialize *each* slave PIC by writing ICW's in the following sequence: ICW1, ICW2, ICW3, and ICW4. Write OCW's as necessary to mask unwanted interrupts, alter priority or read registers.

d. Enable system interrupts by executing an STI (Set Interrupt Flag) instruction.

NOTE

Each PIC independently operates in the fully nested mode (Section 3-29) unless programmed otherwise by ICW4.

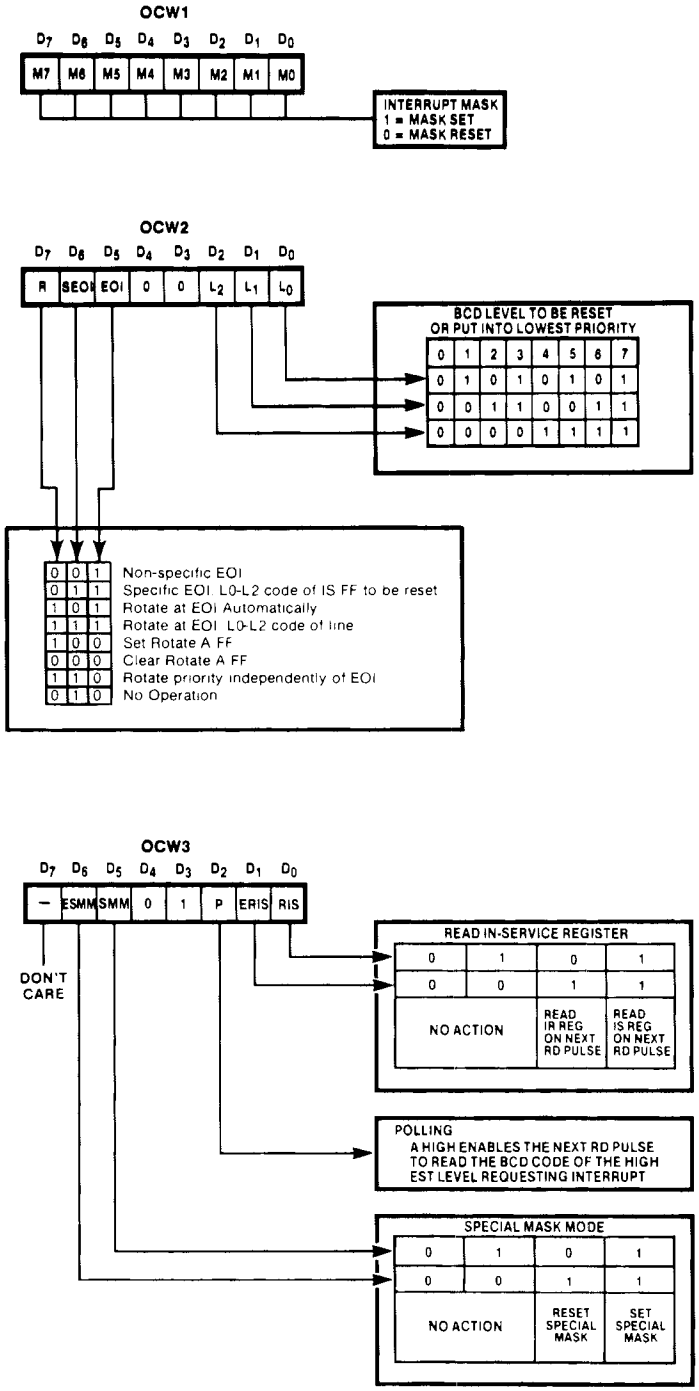


Figure 3-14. PIC Operation Control Word Formats

Table 3-22. Typical PIC Initialization Subroutine (NBV Mode)

```
;INT59 INITIALIZES THE PIC. A 32-BYTE ADDRESS BLOCK BEGINNING WITH
;00020H IS SET UP FOR INTERRUPT SERVICE ROUTINES.
;PIC MASK IS SET, DISABLING ALL PIC INTERRUPTS.
;PIC IS IN FULLY NESTED MODE, NON-AUTO EOI, SINGLE PIC,
;EDGE TRIGGERED, BUFFERED MODE MASTER.
;USES SMASK; DESTROYS-A.
        PUBLIC  INT59
        EXTRN   SMASK           ;SEE TABLE 3-28

INT59:  MOV     AL,13H
        OUT     0C0H,AL         ;ICW1 TO PIC
        MOV     AL,08H
        OUT     0C2H,AL         ;ICW2 TO PIC
        MOV     AL,0DH
        OUT     0C2H,AL         ;ICW4 TO PIC
        MOV     AL,0FFH
        CALL    SMASK
        RET

        END
```

Table 3-23. Typical Master PIC Initialization Subroutine (BV Mode)

```
;INTMA INITIALIZES MASTER PIC WITH A SINGLE SLAVE ATTACHED
;TO THE 5 LEVEL INTERRUPT INPUT, VECTOR TABLE FOR MASTER
;PIC IS AT 0020H.
;PIC MASK IS SET WITH ALL PIC INTERRUPTS DISABLED.
;MASTER PIC IS IN SPECIAL FULLY NESTED, NON-AUTO EOI, EDGE TRIGGERED,
;BUFFERED MODE.
;USES SMASK; DESTROYS AL.
        PUBLIC  INTMA
        EXTRN   SMASK           ;SEE TABLE 3-28

INTMA:  MOV     AL,11H          ;ICW1
        OUT     0C0H,AL
        MOV     AL,08H          ;ICW2
        OUT     0C2H,AL
        MOV     AL,20H          ;ICW3
        OUT     0C2H,AL
        MOV     AL,1DH          ;ICW4
        OUT     0C2H,AL
        MOV     AL,0FFH
        CALL    SMASK
        RET

        END
```

Table 3-24. Typical Slave PIC Initialization Subroutine (BV Mode)

```
;INTSL INITIALIZES A SLAVE PIC LOCATED AT ADDRESS BLOCK
;BEGINNING WITH 00040H.
;PIC IS FULLY NESTED, NON-AUTO EOI, EDGE TRIGGERED, BUFFERED MODE.
;PIC IS IDENTIFIED AS SLAVE 5.
;USES-SETI, DESTROYS-AL.

        PUBLIC  INTSL

INTSL:  MOV     AL,11H          ;ICW1
        OUT     0C0H,AL
        MOV     AL,10H          ;ICW2
        OUT     0C2H,AL
        MOV     AL,05H          ;ICW3
        OUT     0C2H,AL
        MOV     AL,09H          ;ICW4
        OUT     0C2H,AL
        RET

        END
```

3-39. OPERATION

After initialization, the master PIC and slave PIC's can independently be programmed at any time by an Operation Command Word (OCW) for the following operations:

a. Auto-rotating priority.
b. Specific rotating priority.
c. Status read of Interrupt Request Register (IRR).
d. Status read of In-Service Register (ISR).
e. Interrupt mask bits are set, reset, or read.
f. Special mask mode set or reset.

Table 3-25 lists details of the above operations. Note that an End-of-Interrupt (EOI) or a Specific End-of-Interrupt (SEOI) command is required at the end of each interrupt service routine to reset the ISR (unless in auto EOI). The EOI command is used in the fully nested and autorotating priority modes and the SEOI command, which specifies the bit to be reset, is used in the specific rotating priority mode. Tables 3-26 through 3-30 provide typical subroutines for the following:

a. Read IRR (Table 3-26).
b. Read ISR (Table 3-27).
c. Set mask register (Table 3-28).
d. Read mask register (Table 3-29).
e. Issue EOI command (Table 3-30).

Table 3-25. PIC Operation Procedures

Operation	Procedure
Auto-Rotating Priority Mode	To set Auto-Rotating mode with AEOI (requires AEOI to be set in ICW1): In OCW2, write a *Rotate in Automatic EOI* mode (set) command (80H) to Port 00C0H. To clear Auto-Rotating mode, with AEOI: In OCW2, write a *Rotate in Automatic EOI* (clear) mode command (00H) to Port 00C0H. To terminate interrupt and rotate priority (non Auto EOI mode): (AEOI not set in ICW1) In OCW2, write a *Rotate on non-specific EOI* command (0A0H) to Port 00C0H.
Specific Rotating Priority Mode	To rotate/set priority without EOI D7 D6 D5 D4 D3 D2 D1 D0 1 1 0 0 0 L2 L1 L0 Binary value of lowest priority IR line To terminate interrupt (EOI) and rotate/set priority D7 D6 D5 D4 D3 D2 D1 D0 1 1 1 0 0 L2 L1 L0 Binary value of IR level to be reset *and* IR line to be lowest priority.

Table 3-25. PIC Operation Procedures (Continued)

Operation	Procedure
Interrupt Request Register (IRR) Status	The IRR stores a "1" in the associated bit for each IR input line that is requesting an interrupt. To read the IRR (refer to footnote): (1) Write 0AH to Port 00C0. (Write OCW3) (2) Read Port 00C0. Status is as follows: D7 D6 D5 D4 D3 D2 D1 D0 IR Line: 7 6 5 4 3 2 1 0
In-Service Register (ISR) Status	The ISR stores a "1" in the associated bit for priority inputs that are being serviced. The ISR is updated when an EOI command is issued. To read the ISR (refer to footnote): (1) Write 0BH to Port 00C0. (Write OCW3) (2) Read Port 00C0. Status is as follows: D7 D6 D5 D4 D3 D2 D1 D0 IR Line: 7 6 5 4 3 2 1 0
Interrupt Mask Register	To set mask bits in OCW1, write the following mask byte to Port 00C2: D7 D6 D5 D4 D3 D2 D1 D0 IR Bit Mask: M7 M6 M5 M4 M3 M2 M1 M0 1 = Mask Set (inhibited) 0 = Mask Reset (enabled) To read mask bits, read Port 00C2.
Special Mask Mode	The Special Mask Mode enables lower level interrupts than the one in service. To set, write 68H to Port 00C0. To reset, write 48H to Port 00C0.
NOTE: If previous operation was addressed to same register, it is not necessary to rewrite the OCW.	

Table 3-26. Typical PIC Interrupt Request Register Read Subroutine

```
;RR0 READS PIC INTERRUPT REQUEST REG.
;DESTROYS-AL.

        PUBLIC  RR0

RR0:    MOV     AL,0AH          ;OCW3 RR INSTRUCTION TO PIC
        OUT     0C0H,AL
        IN      AL,0C0H
        RET

        END
```

Table 3-27. Typical PIC In-Service Register Read Subroutine

```
;RISO READS PIC IN-SERVICE REGISTER.
;DESTROYS-A.

            PUBLIC    RISO

RISO:       MOV       AL,0BH          ;OCW3 RIS INSTRUCTION TO PIC
            OUT       0C0H,AL
            IN        AL,0C0H
            RET

            END
```

Table 3-28. Typical PIC Set Mask Register Subroutine

```
;SMASK STORES AL REG INTO PIC MASK REG.
;A ONE MASKS OUT AN INTERRUPT, A ZERO ENABLES IT.
;USES-AL, DESTROYS-NOTHING. CALLING ROUTINE PLACES MASK
;IN AL REGISTER BEFORE CALLING SMASK.
            PUBLIC    SMASK

SMASK:      OUT       0C2H,AL
            RET

            END
```

Table 3-29. Typical PIC Mask Register Read Subroutine

```
;RMASK READS PIC MASK REG INTO AL REG.
;DESTROYS-AL.

            PUBLIC    RMASK

RMASK:      IN        AL,0C2H
            RET

            END
```

Table 3-30. Typical PIC End-Of-Interrupt Command Subroutine

```
;EOI ISSUES END-OF-INTERRUPT TO PIC.
;DESTROYS-AL.

            PUBLIC    EOI

EOI:        MOV       AL,20H          ;NON-SPECIFIC EOI
            OUT       0C0H,AL
            RET

            END
```

3-40. 8088 INTERRUPT HANDLING

The 8088 CPU has two interrupt input request lines: Interrupt Request (INTR) and Non-Maskable Interrupt Request (NMI). All of the interrupt requests handled by the 8259A interrupt controller are passed to the 8088 CPU via the INTR line. The NMI input on the iSBC 88/25 board is not used in the factory default configuration, but can be reconfigured. Refer to Section 2-16 for complete jumper instructions.

Section 3-41 provides a summary of the NMI input functions and Section 3-42 summarizes INTR functions. For a complete discussion of 8088 interrupt handling, refer to the Intel *Component Data Catalog*, and Intel *Application Note AP-59*.

3-41. NON-MASKABLE INTERRUPT (NMI)

The NMI input has the higher priority of the two interrupt inputs. A low-to-high transition on the NMI input will be serviced at the end of the current instruction or between whole moves of a block type instruction. The worst case response to NMI is during a multiply, divide, or variable shift instruction.

When the NMI input is active, the CPU performs the following:

a. Pushes the flag registers into the stack (same as PUSHF).

b. Clears the Interrupt Flag (same as CLI). This disables all maskable interrupts.

c. Transfers control with an indirect call through vector location 00008.

The NMI input is intended mainly for catastrophic error handling, such as a system power failure interrupt. Upon completion of the service routine, the CPU automatically, restores the flags and returns to the main program.

3-42. MASKABLE INTERRUPT (INTR)

The INTR input has the lower priority of the two interrupt inputs. A high level on the INTR input will be serviced at the end of the current instruction or at the end of a whole move for a block-type instruction.

When INTR goes active, the CPU performs the following (assuming the Interrupt Flag is set):

a. Issues two acknowledge signals; upon receipt of the second acknowledge signal, the interrupting device (master or slave PIC) will respond with a one-byte interrupt identifier.

b. Pushes the Flag registers onto the stack (same as a PUSHF instruction).

c. Clears the Interrupt Flag, thereby disabling further maskable interrupts.

d. Multiples by four (4) the binary value (X) contained in the one-byte identifier from the interrupting device.

e. Transfers control with an indirect call through location 4X.

Upon completion of the service routine, the CPU automatically restores its flags and returns to the main program.

3-43. MASTER PIC BYTE IDENTIFIER. The master (on-board) PIC responds to the second acknowledge signal from the CPU only if the interrupt request is from a non-slaved device; i.e., a device that is connected directly to one of the master PIC IR inputs. The master PIC has eight IR inputs numbered IR0 through IR7, which are identified by a 3-bit binary number. ICW2 determines the five most significant bits of the interrupt type passed to the 8088 CPU. Thus, if an interrupt request occurs on IR5, and ICW2 was written with a value of 20H (Table 3-24), the master PIC resopnds to the second acknowledge signal from the CPU by outputting the byte 00100101_2 (25_{16}). The CPU multiples this value by four and transfers control with an indirect call through 10010100_2 (94_{16}).

3-44. SLAVE PIC BYTE IDENTIFIER. Each slave PIC is initialized with a 3-bit identifier (ID) in ICW3. The slave PIC requests an interrupt by driving the associated master PIC IR line. The master PIC, in turn, drives the CPU INTR input high and the CPU outputs the first of two acknowledge signals. In response to the first acknowledge signal, the master PIC outputs a 3-bit binary code to slaved PIC's via the cascade lines; this 3-bit code allows the appropriate slave PIC to respond to the second acknowledge signal from the CPU.

Assume that the slave PIC has the ID code 111, assigned in ICW3 that the ICW2 was programmed with a value of 40_{16}, and that the device requesting service is driving the IR2 line of the slave PIC (010). Thus, in response to the second acknowledge signal, where the slave PIC has previously put its ID code 111_2 on its cascade lines, the slave PIC outputs 01000010_2 (42_{16}). The CPU multiples this value by four and transfers control with an indirect call through 100001000_2 (108_{16}).

CHAPTER 4
PRINCIPLES OF OPERATION

4-1. INTRODUCTION

This chapter provides a brief description of each major iSBC 88/25 functional block. Some references to on-board circuitry and signals are provided where such detail is required. The descriptions in this chapter do not attempt to provide the reader with a complete detailed description of the entire board in all operating modes; similarly, this chapter does not attempt to describe the internal operation of each LSI device on the iSBC 88/25 board. Rather, this chapter is intended to expand on the material presented in previous chapters. Additional information on Intel LSI devices is provided in the *Intel Data Catalog*, the *Intel Peripheral Design Handbook*, and the *Intel 8086 Family User's Manual*. Multibus information is provided in the *Intel Multibus Specification*. Additional information on the iSBX bus is provided in the *Intel iSBX Bus Specification*. Order numbers for all referenced literature are listed in the Preface of this manual.

4-2. MAJOR FUNCTIONAL BLOCKS

The iSBC 88/25 board is composed of eleven major functional areas as listed below and shown in Figure 4-1. Sections 4-3 through 4-13 provide descriptions of the major functional areas listed here.

iSBC 88/25 Board Major Functional Blocks:

- 8088 Processor
- Address Decoding
- Read-Only Memory (ROM)
- Serial Port Interface
- Interrupt Controller
- iSBX Multimodule Interface
- Timing Circuitry
- Random Access Memory (RAM)
- Interval Timer
- Parallel Port Interface
- Multibus Interface

4-3. 8088 PROCESSOR

The central processor for the iSBC 88/25 board is Intel's 8088 Microprocessor (referred to hereafter as CPU or central processing unit) operating at 5 MHz. The CPU architecture includes four 16-bit byte addressable data registers, two 16-bit memory base pointer registers, and two 16-bit index registers. All registers are accessed by a total of 24 operand addressing modes for comprehensive memory addressing and for high level language and assembly language data structure support.

The 8088 instruction repertoire includes variable length instruction format (including double operand instructions), 8-bit and 16-bit signed and unsigned arithmetic operators for binary, BCD and unpacked ASCII data, and iterative word and byte string manipulation functions. Additional information on 8088 CPU timing and instruction set is available in the *Intel 8086 Family User's Manual*, and the *Intel Data Catalog*.

For enhanced numeric processing capability, the iSBC 337 Numeric Data Processor Multimodule option extends the 8088 CPU architecture and data set. Over 60 numeric instructions offer arithmetic, trigonometric, transcendental, logarithmic, and exponential functions. Supported data types include 16, 32, and 64-bit integer, and 32 and 64-bit floating point, 18-digit packed BCD and 80-bit temporary. Additional information on the iSBC 337 Numeric Data Processor is available in the *Intel 8086 Family User's Manual Numerics Supplement*.

4-4. ON-BOARD TIMING

On-board timing for the CPU is provided by an 8284A Clock Generator and Driver device. This device employs a 15 MHz crystal and outputs 5 MHz for the CPU clock input. The RESET and READY functions are also generated by the 8284A device.

A substitute device is jumpered into operation if the iSBC 337 Numeric Data Processor option is installed. This device is an 8224 oscillator used to provide 4.17 MHz to the CPU clock input.

A third group of timing circuitry consisting of another 8224 oscillator and two 4-bit counter devices, generates clock signals for the 8253 Interval Timer device and produces BCLK/ and CCLK/ Multibus clock signals (9.83 MHz).

The 8253 Programmable Interval Timer is used to generate timing for the serial port (baud rate clock), and generates inputs to the interrupt controller.

4-5. RANDOM ACCESS MEMORY (RAM)

The board is supplied with two 2168 devices installed at U67 and U51. These devices correspond to the lowest RAM locations, from address 00000 to 00FFF (Hex). Each device provides 4K X 4-bits of storage.

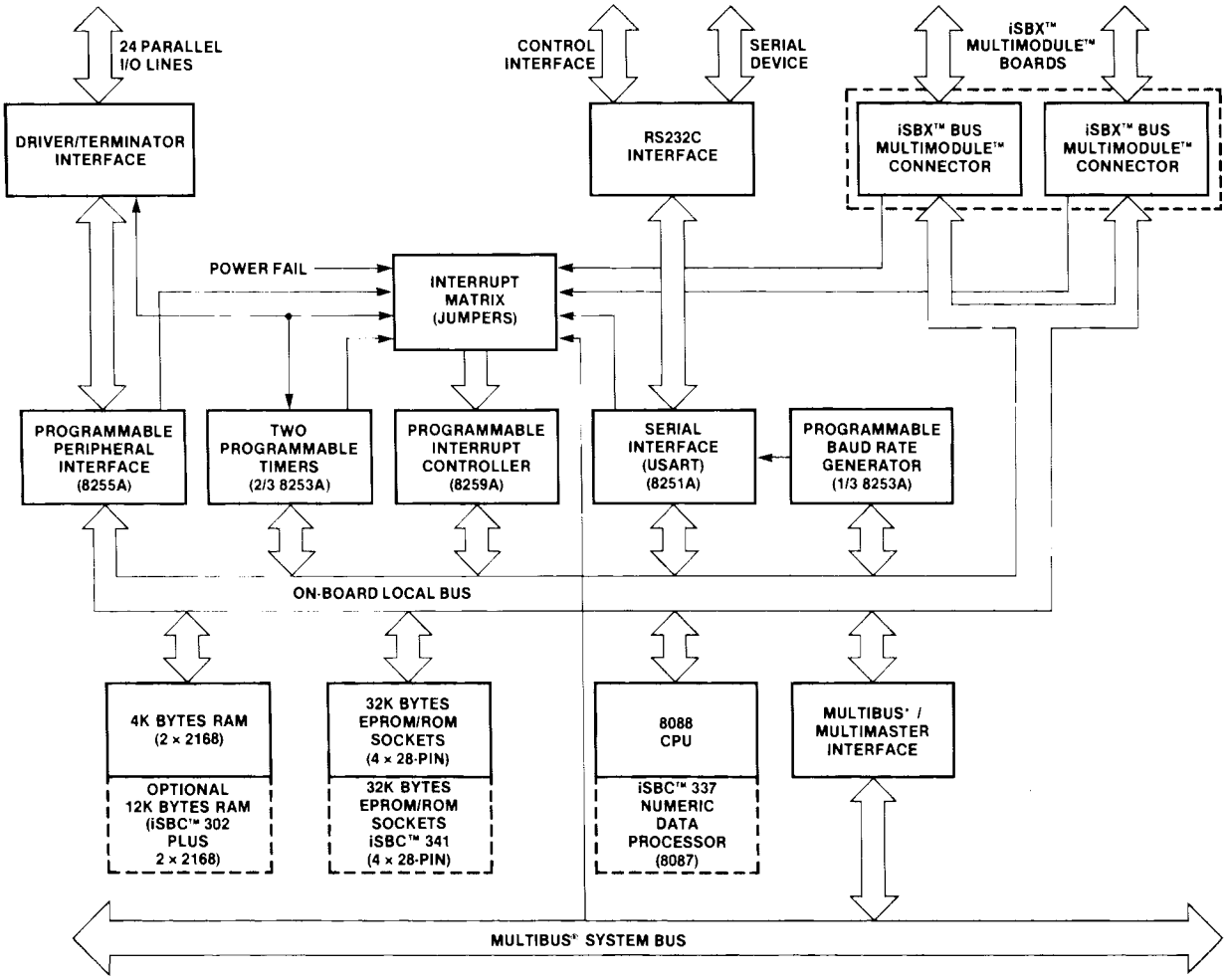


Figure 4-1. iSBC 88/25™ Block Diagram

Additional on-board RAM expansion may be accomplished by installing the optional iSBC 302 RAM Expansion Module. Section 2-10 provides instructions for installation. With this option installed, total on-board RAM increases to 12K (or 16K) bytes with six (or eight) RAM devices installed, or locations 00000 to 02FFF (or 03FFF) (Hex).

All on-board RAM (including iSBC 302 RAM) is accessed by the 8088 CPU without wait states, yielding a memory cycle time of 800 nanoseconds.

The so called "Byte-Wide" RAM devices may also reside on the iSBC 88/25 board. These 28-pin devices are installed into ROM sockets U34 and U65 and are addressed accordingly (see Section 3-2).

4-6. READ-ONLY MEMORY (ROM)

The iSBC 88/25 board has four sockets for use with ROM devices. The board is compatible with four sizes of ROM devices. These are summarized in Section 2-7. The board's default configuration is for 24-pin, 2K byte X 8-bit devices. ROM addressing ranges depend on the size of the device and the number of devices installed. Table 2-1 specifies the address range for each socket, according to device size.

The iSBC 341 ROM Expansion Module plugs directly into board sockets U34 and U65.

4-7. ADDRESS DECODING

When the 8088 processor issues an address it also outputs several status bits which are decoded by on-board circuitry to indicate whether the address is a

memory location or an I/O location. The signal MEM (IO/) is produced by this circuitry to indicate whether the address should be examined by the memory decode circuitry or by the I/O decode circuitry. When MEM (IO/) is a "1" memory is indicated: conversely, when MEM (IO/) is a "0" an I/O device is indicated.

Address decoding is accomplished through two preprogrammed PROMs. The memory decode PROM resides in socket U70; the I/O decode PROM resides in socket U69. Memory address decoding is discussed in Section 4-8; I/O address decoding is discussed in Section 4-9.

4-8. MEMORY ADDRESS DECODING

Memory address decoding is accomplished at three separate levels. The first level is the selection of the desired 128K byte page within a 1M byte space. This is programmed by jumper selection and by decoding the address lines A17, A18, and A19 at decoder U41. The factory default page for RAM is set at location 00000 to a maximum of 1FFFF (Hex); for ROM the default page is set at location E0000 to FFFFF. Refer to Section 2-9 for page select jumper instructions.

The second level of memory address decoding is accomplished with the memory decode PROM in socket U70. This device is preprogrammed at the factory to determine if the current address is an on-board location and to enable the proper RAM or ROM chip select (CS/) signal if the address is on-board. The decode PROM evaluates address lines A11 through A17. The signal ON BD ADR/ will be true if the address is on-board. One of four RAM chip select signals (RAM0/ through RAM3/) will be enabled if the address is in the RAM page. Each RAM chip select signal enables two RAM devices (each device stores half of the addressed byte). One of the eight ROM chip select signals (PROM0/ - PROM7/) will be enabled if the address is in the ROM page. If the current address is an off-board address, the signal ON BD ADR/ will be false and no memory chip select signals are enabled on the iSBC 88/25 board. Appendix A provides a decode PROM memory map and truth table.

The third level of address decoding occurs at the RAM or ROM device. The RAM devices examine address lines A0 through A11; ROM devices examine lines A0 through A13.

4-9. I/O ADDRESS DECODING

The I/O decode circuitry examines address lines A0 and A3-A15 to determine if the address is a valid on-board I/O address and to enable the proper chip select signal. If the address is a valid on-board address, the signal ON BD ADR/ will be true; conversely if not a valid on-board address, the signal will be false.

I/O addressing is discussed in Section 3-3. When the 8088 CPU issues an I/O address, through decoding logic in the I/O decode PROM and other circuitry one of eight chip select signals is enabled. Each signal corresponds to one of the on-board I/O devices:

8251A CS/
8253A CS/
8255A CS
8259A CS/
SBX2 CS0/
SBX2 CS1/
SBX1 CS0/
SBX1 CS1/

Notice that each SBX location has two chip select signals. Both signals may not necessarily be used on all iSBX Multimodule boards. Refer to the iSBX board reference manual for exact addressing.

4-10. 8253-5 INTERVAL TIMER

This device resides in socket U23. The device consists of three software selectable counters. Each counter has its own input pin and output in. Input frequencies are determined by jumper selection. The board's default configuration for the inputs is as follows:

CLK0 Input	1.23 MHz
CLK1 Input	153.6 KHz
CLK2 Input	1.23 MHz

Section 2-9 provides instructions for alternative jumper input selections. All inputs must be 2.0 MHz or less.

The three timer outputs are each routed to various board devices via jumper connections. Output 2 is connected to the TxC and RxC clock inputs of the 825A Programmable Communications Interface device (USART) in socket U24. Output 1 is connected to jumper post 111 of the interrupt source matrix. This post is not wired to the interrupt controller in the default configuration. Output 0 is connected to jumper post 112 of the interrupt source matrix. This post is jumpered to interrupt level 2 (IR2) on the 8259A Interrupt Controller in the factory default configuration.

The complete functional definition of the interval timer is programmed by system software. A set of control words must be sent out by the CPU to initialize each counter with the desired mode and quantity information. Each counter consists of a single, 16-bit, presettable, down-counter. The counter can operate in either binary or BCD and its input gate and output are configured by the selection of modes stored in the control word register. Refer to Chapter 3 for additional programming information. Complete PIT information is provided in the *Intel Data Catalog.*

4-11. SERIAL PORT CIRCUITRY

The iSBC 88/25 board utilizes an Intel 8251A Programmable Communications Interface (PCI) device to handle serial communications through connector J2. On board jumpers are used to select the clock source for transmission and reception. The device is configured as a data set, for RS-232 communications protocol.

The complete functional definition of the PCI is programmed by system software. A set of control words must be sent out by the CPU to initialize the PCI to support the desired communications format. These control words will program the baud rate, character length, number of stop bits, synchronous or asynchronous operation, even/odd parity and other parameters. In the synchronous mode, options are also provided to select either internal or external character synchronization.

Once programmed, the PCI is ready to perform its communications functions. The TxRDY output is raised high to signal the CPU that the PCI is ready to receive a data character from the CPU. This output (TxRDY) is reset automatically when the CPU writes a character into the PCI. When the PCI receives serial data from a modem or I/O device, the RxRDY output is raised high to signal the CPU that the PCI has a complete character for the CPU to fetch. RxRDY is reset automatically upon the CPU data read operation. The PCI cannot begin transmission until the Tx Enable bit is set in the Command Instruction byte, and it has received a Clear To Send (CTS/) input. The TxD output will be held in the marking state upon reset.

Refer to Chapter 3 for additional programming information. Complete PCI information is provided in the *Intel Data Catalog.*

4-12. PARALLEL PORT INTERFACE

The iSBC 88/25 board has 24 programmable parallel I/O lines implemented with a single Intel 8255A Programmable Peripheral Interface (PPI) device in socket U22. The lines are grouped into three software programmable 8-bit I/O ports. On-board usage of each line is variable, depending on mode selection and jumper status. Section 2-16 provides parallel port jumper configurations. Device programming is discussed in Section 3-22.

There are three basic modes of operation which can be selected by system software:

Mode 0 — Basic Input/Output

Mode 1 — Strobed Input/Output

Mode 2 — Bi-Directional Bus

When the reset input gate goes high all ports in the 8255A will be set to the input mode (i.e., all 24 lines will be in the high impedance state). After the reset is removed, the 8255A can remain in the input mode with no additional initialization required. During the execution of the system program any other modes may be selected using a single output instruction.

The modes for port A and B can be separately defined, while port C is divided into two portions as required by the port A and port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be tailored to almost any I/O structure.

Any of the eight port C bits can be set or reset using a single output instruction. When port C is being used as status/control for port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.

For additional 8255A PPI information refer to the *Intel Peripheral Design Handbook,* or the *Intel Data Catalog.*

4-13. INTERRUPT CONTROL AND TIMING

Interrupt circuitry on the iSBC 88/25 board consists of an interrupt source jumper matrix, an 8259A Programmable Interrupt Controller (PIC), and interrupt acknowledge logic. The board can experience three basic types of interrupts: a direct CPU input nonmaskable interrupt (NMI); an on-board interrupt through the PIC; and off-board, Multibus vectored interrupts. Off-board Multibus vectored interrupts may be cascaded from other PIC devices.

Multibus vectored interrupts require additional response time as compared to on-board interrupts. For this reason Multibus vectored interrupts are not allowed to the iSBC 88/25 board in its factory default configuration. A jumper connection is required to be removed to enable this feature (refer to Section 2-20). If enabled, wait states are automatically inserted by the board to allow proper timing.

A typical non-bus-vectored interrupt operation is as follows: assume that an interrupt is initiated by an on-board function, driving the IR5 line of the PIC high. If no higher interrupt is in progress, the PIC drives the INTR signal high. Assuming that the NMI interrupt is not active and the CPU interrupt enable flip-flop is set, the CPU suspends current operations and proceeds with the first of two back-to-back INTA cycles.

In the default configuration (Non BVI), the local 8288 bus command decoder (U44) drives the INTA/ line low. On receipt of the first INTA/ signal the PIC

stores the internal state of its priority resolution logic. This signal also produces LOCAL INTA/ 2 which is used to gate two wait states into the READY circuitry. The Multibus arbitration circuitry is inhibited from requesting the Multibus lines during this time.

The CPU then proceeds to the second INTA/ cycle. On receipt to the second INTA/ signal, the PIC places an 8-bit identifier for IR5 on the internal board data bus. This is read by the CPU and interrupt timing is terminated.

The CPU multiplies the 8-bit identifier by four to derive the restart address of the interrupting device. After the service routine is completed, the CPU automatically resets all its affected flags and returns to the main program.

4-14. MULTIBUS INTERFACE

The Multibus interface is the system interface. The iSBC 88/25 board communicates with other boards in the system over the Multibus lines. The Multibus lines adhere to a design standard, as specified in the *Intel Multibus Specification*, and as summarized in Table 2-20.

In a typical application, the iSBC 88/25 board would be a master board in the system. This means the iSBC 88/25 board could perform Multibus arbitration with all boards in the system. Each board would have a specific priority as controlled by board placement and jumper selection. Refer to Section 2-24 for a complete discussion of Multibus arbitration.

Multibus control circuitry includes the Bus Arbiter device (U56), two bus command decoders (U44 and U57), bi-directional data bus and address bus drivers (U46, 48, 58, 60, 61, 63, and 66), and interrupt driver/receivers (U59). The Bus Arbiter allows the iSBC 88/25 board to operate as a bus master in the system in which the 8088 CPU can request the Multibus lines when a resource is required. Multibus timing for the iSBC 88/25 board is discussed in Chapter 2.

4-15. iSBX MULTIMODULE INTERFACE

Essentially, the iSBX bus is an extension of the local on-board iSBC 88/25 internal bus. This bus is interfaced to optional plug-in modules with a single iSBX connector. Two such connectors reside on the iSBC 88/25 board (J3 and J4). All necessary power lines, data lines, address lines, and control lines are routed through the two iSBX connectors. The 8088 processor treats the iSBX board as another on-board I/O location. Addressing is discussed in Section 3-3. Pin assignments and signal descriptions for the iSBX connectors are given in Chapter 2. For additional iSBX Multimodule information, refer to the *Intel iSBX Bus Specification.*

CHAPTER 5
SERVICE INFORMATION

5-1. INTRODUCTION

This chapter provides the following service related information:

a. Repair assistance information.

b. Replacement parts list and diagram,

c. Jumper post location diagram.

d. Schematic diagrams.

5-2. SERVICE AND REPAIR ASSISTANCE

United States customers can obtain service and repair assistance by contacting the Intel Product Service Hotline in Phoenix, Arizona. Customers outside the United States should contact their sales source (Intel Sales Office or Authorized Distributor) for service information and repair assistance.

Before calling the Product Service Hotline, you should have the following information available:

a. Date you received the product.

b. Complete part number of the product (including dash number). On boards, this number is usually silk-screened onto the board. On other products, it is usually stamped on a label.

c. Serial number of product. On boards, this number is usually stamped on the board. On other products, the serial number is usually stamped on a label.

d. Shipping and billing addresses.

e. If your Intel product warranty has expired, you must provide a purchase order number for billing purposes.

f. If you have an extended warranty agreement, be sure to advise the Hotline personnel of this agreement.

Use the following numbers for contacting the Intel Product Service Hotline:

Telephone

All U.S. locations,
Except Alaska, Arizona, & Hawaii:

(800) 528-0595

All other locations: (602) 869-4600

TWX Number

910 - 951 - 1330

Always contact the Product Service Hotline before returning a product to Intel for repair. You will be given a repair authorization number, shipping instructions, and other important information which will help Intel provide you with fast, efficient service. If you are returning the product because of damage sustained during shipment or if the product is out of warranty, a purchase order is required before Intel can initiate the repair.

In preparing the product for shipment to the Repair Center, use the original factory packing material, if possible. If this material is not available, wrap the product in a cushioning material such as Air Cap TH-240, manufactured by the Sealed Air Corporation, Hawthorne, N.J. Then enclose in a heavy duty corrugated shipping carton, and label "FRAGILE" to ensure careful handling. Ship only to the address specified by Product Service Hotline personnel.

5-3. REPLACEMENT PARTS

A complete list of replacement parts is provided in Table 5-1. This list provides the part number, description and quantity of the item. Notice that each item is referenced in the parts location diagram. Figure 5-1 shows the location of each iSBC 88/25 referenced part in Table 5-1. Figures 5-3 and 5-5 show the location of the iSBC 341 ROM Expansion Module parts and the iSBC 302 RAM Expansion Module parts.

5-4. SERVICE DIAGRAMS

The following schematic diagrams are included in this chapter:

Figure 5-2 iSBC 88/25 Board

Figure 5-4 iSBC 341 ROM Expansion Module

Figure 5-6 iSBC 302 RAM Expansion Module

Notice that a functional description of each jumper connection on a particular schematic sheet is referenced to the left of the fold out sheet.

The schematic diagrams are current when the manual is printed. However, minor revisions to the diagrams may occur between manual printings. Therefore, Intel provides photocopies of the current schematic diagrams with the board, when it is shipped from the factory. These diagrams should be inserted into this manual for future reference. In most instances, the diagrams shipped with the board will be identical to those printed in the manual.

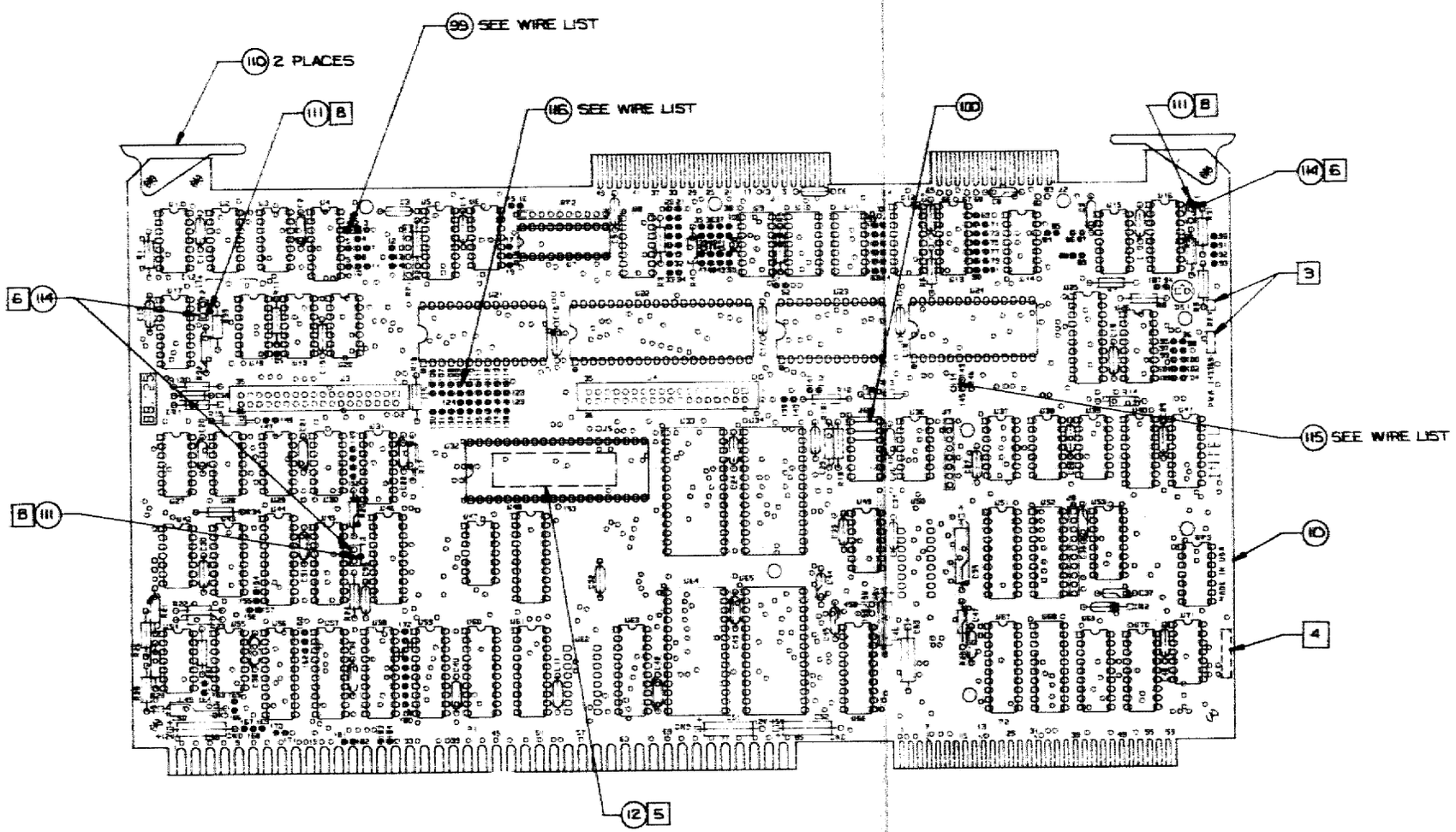
Table 5-1. iSBC 88/25™ Replacement Parts List

Part No.	Description	Ref. Des.	Qty
143383-001	I/O Decode PROM	U69	1
144011-001	Memory Decode PROM	U70	1
3002044-01	Socket, 1-pin	J5	1
3002044-08	Socket, 8-pin	J7	1
3002044-10	Socket, 10-pin	J8	1
101194-002	I.C. Intel, 8259A	U21	1
101187-002	I.C. Intel, 8224	U14, U16	2
101190-001	I.C. Intel, 8251A	U24	1
101191-002	I.C. Intel, 8253-5	U23	1
101192-003	I.C. Intel, 8255A-5	U22	1
101201-001	I.C. Intel, 8286	U25	1
101202-001	I.C. Intel, 8287	U7, 63	2
101203-001	I.C. Intel, 8288	U44, 57	2
101204-001	I.C. Intel, 8289	U56	1
104112-001	I.C. Intel, 8088	U32	1
104227-002	I.C. Intel, 8284A	U45	1
104462-001	I.C. Intel, 2168R	U51, 67	2
100600-021	I.C., 74S00	U1, 18, 37	3
100600-031	I.C., 74LS00	U30, 49	2
100602-021	I.C., 74S02	U27	1
100604-021	I.C., 74S04	U29, 38	2
100604-031	I.C., 74LS04	U6	1
100606-001	I.C, 7406	U42	1
100608-021	I.C., 74S08	U47, 54, 71	3
100608-031	I.C., 74LS08	U2, 28	2
100610-021	I.C., 74S10	U19, 39	2
100617-021	I.C., 74S112	U43	1
100632-021	I.C, 74S138	U26, 40, 41, 53	4
100622-031	I.C., 74LS123	U5	1
100649-021	I.C., 74S163	U12	1
100649-031	I.C., 74LS163	U13	1
100656-021	I.C., 74S175	U4	1
100668-031	I.C., 74LS240	U58-61	4
100679-021	I.C., 74S260	U36	1
100689-021	I.C., 74S32	U3	1
100694-001	I.C., 8097	U31	1
100696-021	I.C., 74S37	U55	1
100852-001	I.C., 75188	U14	1
100713-031	I.C., 74LS74	U20	1
100853-001	I.C., 75189A	U15	1
100697-021	I.C., 74S373	U46, 48, 66	3
101576-001	CRYSTAL, 15.000 MHz	Y3	1
101576-010	CRYSTAL, 19.6608 MHz	Y1	1
101576-004	CRYSTAL, 12.500 MHz	Y2	1
101655-003	RES., 1K, 1/4W, 5%	R3-6, 8, 15, 16, 27	8
101655-004	RES., 10K, 1/4W, 5%	R1, 11, 12, 13, 18 19, 21, 22, 23, 24	10
101655-005	RES., 100K, 1/4W, 5%	R10, 25	2
101655-069	RES., 240K, 1/4W, 5%	R2	1
101656-030	RES., 510, 1/4W, 5%	R30-33, 20, 24	6
101656-038	RES., 560, 1/4W, 5%	R9, 26	2
101656-039	RES., 5.6K, 1/4W, 5%	R7, 14, 17, 28, 29	5
101655-003	RES., 1K, 1/4W, 5%	R3-6, 8, 15, 16, 27	8
101726-038	R-PAK, 10K, 6 PIN, 3/4W, 2%	RP1	1
101736-038	R-PAK, 10K, 10 PIN, 1.25W, 2%	RP2	1
101740-023	R-PAK, 1K, 14 PIN, 1.5W, 2%	RP3	1
101762-049	CAP, CER., .1uF, 50V, +80-20%	C1-10, 13, 15-22 24-34, 36-45, 47, 48, 54, 55	44
101772-041	CAP, TANT., 22uF, 15V, 10%	C49, 52	2
101773-037	CAP, TANT., 10uF, 15V, 20%	C12, 46, 53	3
101778-035	CAP, TANT., 6.8uF, 35V, 20%	C35	1
101776-033	CAP, TANT., 4.7uF, 20V, 20%	C50, 51	2

Table 5-1. iSBC 88/25™ Replacement Parts List (Continued)

Part No.	Description	Ref. Des.	Qty.
102480-001	PLUG SHORTING, 2 POS		35
103802-001	PLUG SHORTING	J6	3
101563-014	SOCKET, 14 PIN DIP	J6	1
101563-020	SOCKET, 20 PIN DIP	XU52, 68	2
101563-028	SOCKET, 28 PIN DIP	XU33, 34, 64, 65	4
102989-001	SOCKET, 40 PIN DIP	XU32	1
104235-014	SOCKET, 14 PIN DIP	XU8, 9, 10, 11	4
104235-020	SOCKET, 20 PIN DIP	XU7	1
103059-001	CONNECTOR, 36 PIN	J3, 4	2
103019-001	CARD EJECTOR	—	2

REV	DESCRIPTION	BY	DATE	CHK	DATE	APVD
B	ECO 40-2752					
C	ECO 40-2845					



NOTES: UNLESS OTHERWISE SPECIFIED

1. ASSEMBLY PART NUMBER IS 143369-002. THIS DOCUMENT, PL AND WL ARE TRACKING DOCUMENTS.
2. WORKMANSHIP PER 99-0007-001.
3. MARK ASSEMBLY DASH NUMBER AND REVISION LEVEL WITH CONTRASTING PERMANENT COLOR, NON-CONDUCTIVE, .12 HIGH, APPROXIMATELY WHERE SHOWN.
4. MARK ASSEMBLY VENDOR I.D. WITH CONTRASTING PERMANENT COLOR, NON-CONDUCTIVE, .12 HIGH, APPROXIMATELY WHERE SHOWN
5. INSTALL ITEM 12 ON SOLDER SIDE AT U32 SO THAT I.C. PADS ARE FREE OF LABEL AND ADHESIVE.
6. INSULATE CRYSTAL CASE (Y1,Y2,Y3) WITH ITEM 114.
7. SOCKET REFERENCE DESIGNATORS ARE THE I.C. REFERENCE DESIGNATORS PREFIXED WITH "X"

8. INSTALL HEAT SHRINK TUBING (ITEM 114) AROUND CRYSTAL AND WIRE WRAP POST.

QUANTITY PER DASH NO.

UNLESS OTHERWISE SPECIFIED:
1. DIMENSIONS ARE IN INCHES.
2. BREAK ALL SHARP EDGES.
3. DO NOT SCALE DRAWING.
4. TOLERANCES:
ANGLES ±
XX ±
XXX ±

ITEM NO.	DESCRIPTION
	PARTS LIST

SIGNATURE	DATE
DRN BY	4/2/81
CHK BY	4/2/81
ENGR APVD	
APVD	
APVD	

intel

TITLE PRINTED WIRING ASSEM
iSBC 88/25

SIZE	SCLC	CL CODE	FILE LVL	DOCUMENT
D	40	05		1435

SCALE NONE

REV	DESCRIPTION	BY	DATE	CHK	DATE	APVD	DATE
A	ECO 40-2695						

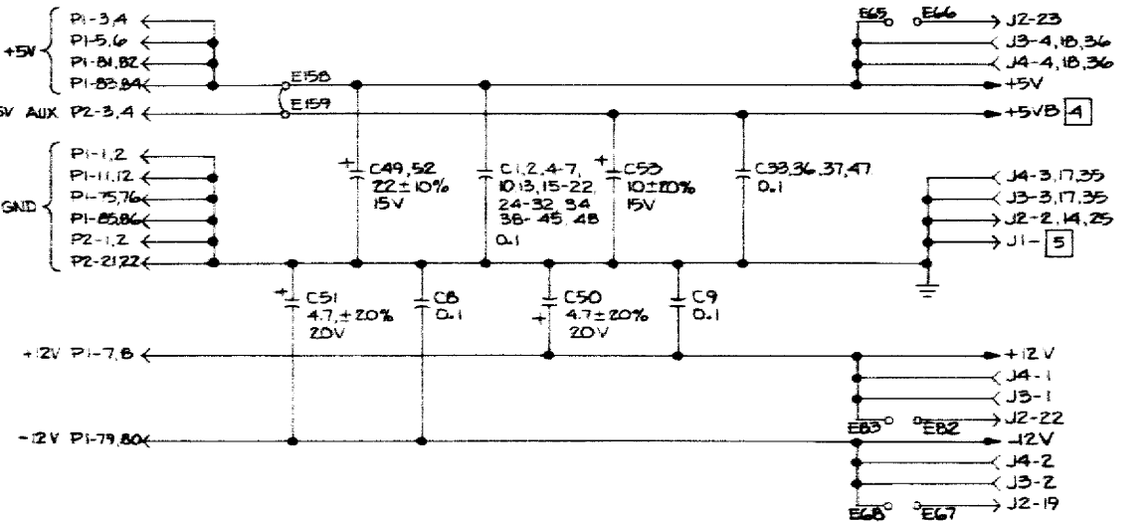


TABLE A		
EPROM SIZE SELECT JUMPERS		
TYPE	DECODE	J6
2716	NONE	1-14, 2-13, 3-12
2732	E90-E91	1-14, 3-12, 6-9
2764	E92-E93	1-14, 6-9
27S4	E90-E91 E92-E93	1-14, 6-9, 7-8

TABLE B		
DEVICE TYPE	PORT NO.	FUNCTION
8251A	D000	DATA
	D002	CONTROL
8253-5	D000	COUNTER 0
	D002	COUNTER 1
	D004	COUNTER 2
	D006	CONTROL
8255A-5	D008	PORT A
	D00A	PORT B
	D00C	PORT C
	D00E	CONTROL
8259A	D010	REG #1
	D012	REG #2

TABLE C		
CLOCK FREQUENCIES		
FREQUENCY	FROM JUMPER	TO JUMPER
1.23 MHz	E53,56,58	E54,55
153.6 KHz	E53,56,58	E57
2.46 MHz	E53,56,58	E61

REF. DESIG.	
LAST USED	NOT USED
U71	U35
Y3	E185, 186
C55	C11, 14, 23
RP3	
R34	
D51	
CR2	
J8	
E187	

POWER, GROUND AND SPARE GATE LOCATOR CHART							
REFERENCE DESIGNATION	DEVICE TYPE	POWER PINS GND	+5V	+12V	-12V	+5VB	SPARE GATES OUTPUT PINS
U51,U67,52,68	2168R	10				20	
U69,70	3625A-1	9	18				
U30	74LS00	7	14				U30-8
U1,18,37	7400	7	14				U8-3,6,8, U37-8
U27	7402	7	14				U27-4,10
U6	74LS04	7	14				
U29,38	7404	7	14				U29-8,U38-4,8,10,12
U42	7406	7	14				U42-4,8
U2,28	74LS08	7	14				U2-3,8, U28-6,11
U47,54,71	7408	7	14				U47-4,11,U54-3,U71-3,11
U19,39	7410	7	14				U39-6,12
U3	7432	7	14				U3-3,11
U55	7437	7	14				U55-11
U20	74LS74	7	14				
U43	74S112	8	16				
U5	74LS123	8	16				U5-13
U26,40,41,53	74S138	8	16				
U13	74LS163	8	16				
U12	74S163	8	16				
U4	74S175	8	16				
U59	74LS240	10	20				
U58,60,61	74S240	10	20				
U56	74S260	7	14				
U46,48,66	74S373	10	20				
U14	75188	7		14	1		
U15	75189	7	14				
U32	8086	1,20	40				
U31	8097	8	16				U31-14
U16,17	8224	8	16				
U24	8251A	4	26				
U23	8253-5	12	24				
U22	8255A-5	7	26				
U21	8259A	14	28				
U45	8284A	9	18				
U25	8286	10	20				
U7,63	8287	10	20				
U44,57	8288	10	20				
U56	8289	10	20				
U49	74LS00	7				14	U49-8
XU8,9,10,11	SOCKET	7	14				
U50,62	SPARE	7,8	16				

ES: UNLESS OTHERWISE SPECIFIED
APACITANCE VALUES ARE IN MICROFARADS, +80% -20%, 50V
ESISTANCE VALUES ARE IN OHMS, 1/4 W, 5%.
LL RESISTOR PAKS ARE 10K.
+5VB" INDICATES BATTERY +5V.
ALL ODD NUMBER PINS ON J1 ARE GROUND.
EPROM SIZE SELECT CONNECTIONS ARE AS SHOWN IN TABLE A.
PORT FUNCTIONS ARE AS SHOWN IN TABLE B.
LOCK FREQUENCIES ARE AS SHOWN IN TABLE C.
U33, U34, U52, U64, U65 AND U68 ARE CUSTOMER INSTALLED.

ITEM NO.	DESCRIPTION
QUANTITY PER DASH NO.	PARTS LIST

UNLESS OTHERWISE SPECIFIED
1. DIMENSIONS ARE IN INCHES.
2. BREAK ALL SHARP EDGES.
3. DO NOT SCALE DRAWING.
4. TOLERANCES: FRACT ±, .X ±, .XXX ±

SIGNATURE	DATE
DRN BY K.O.	2/6/81
CHK BY	2/6/81
ENGR/PROJ LDR	2/6/81
APVD	
APVD	

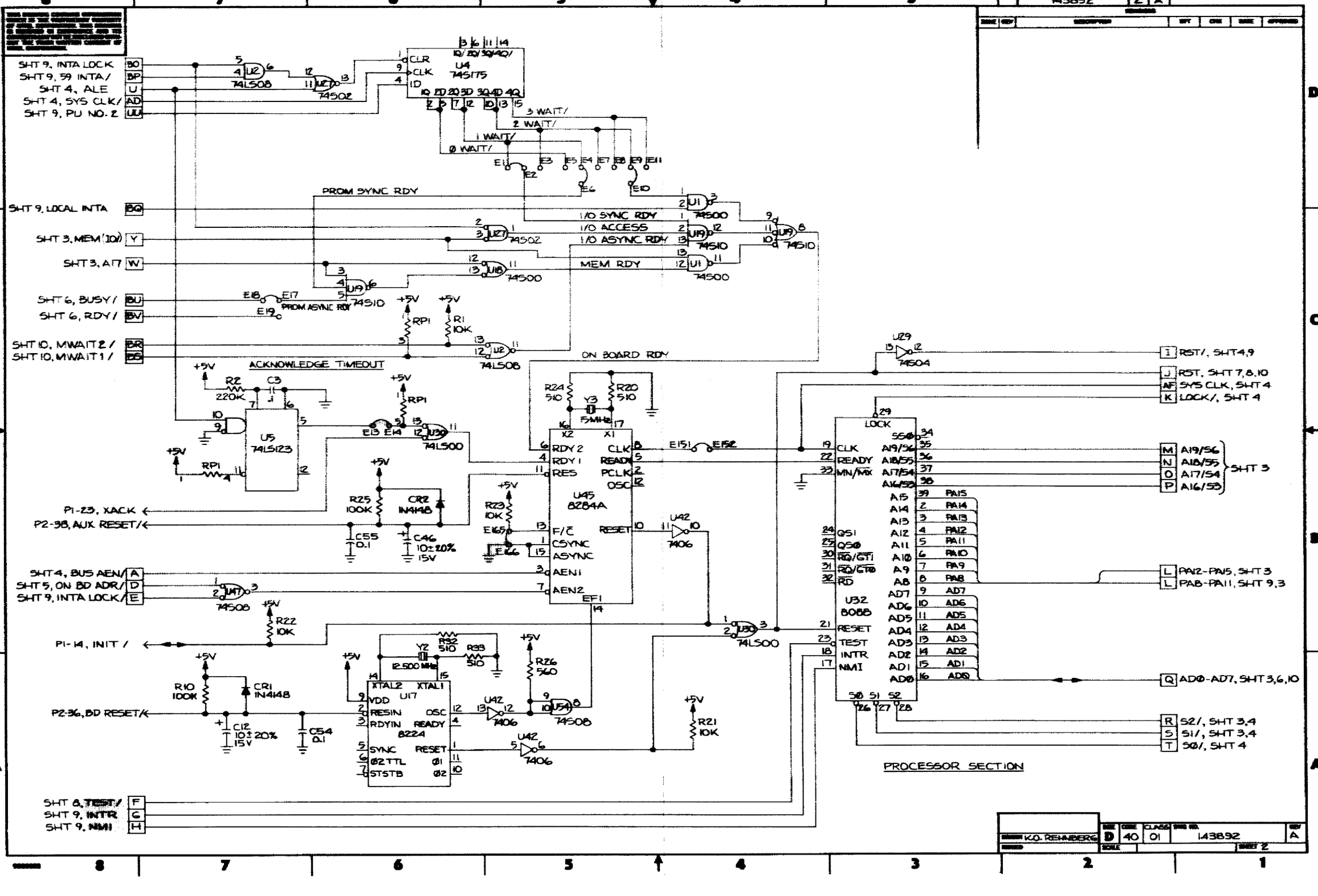
intel 3065 BOWERS AVE SANTA CLARA CALIF. 95051

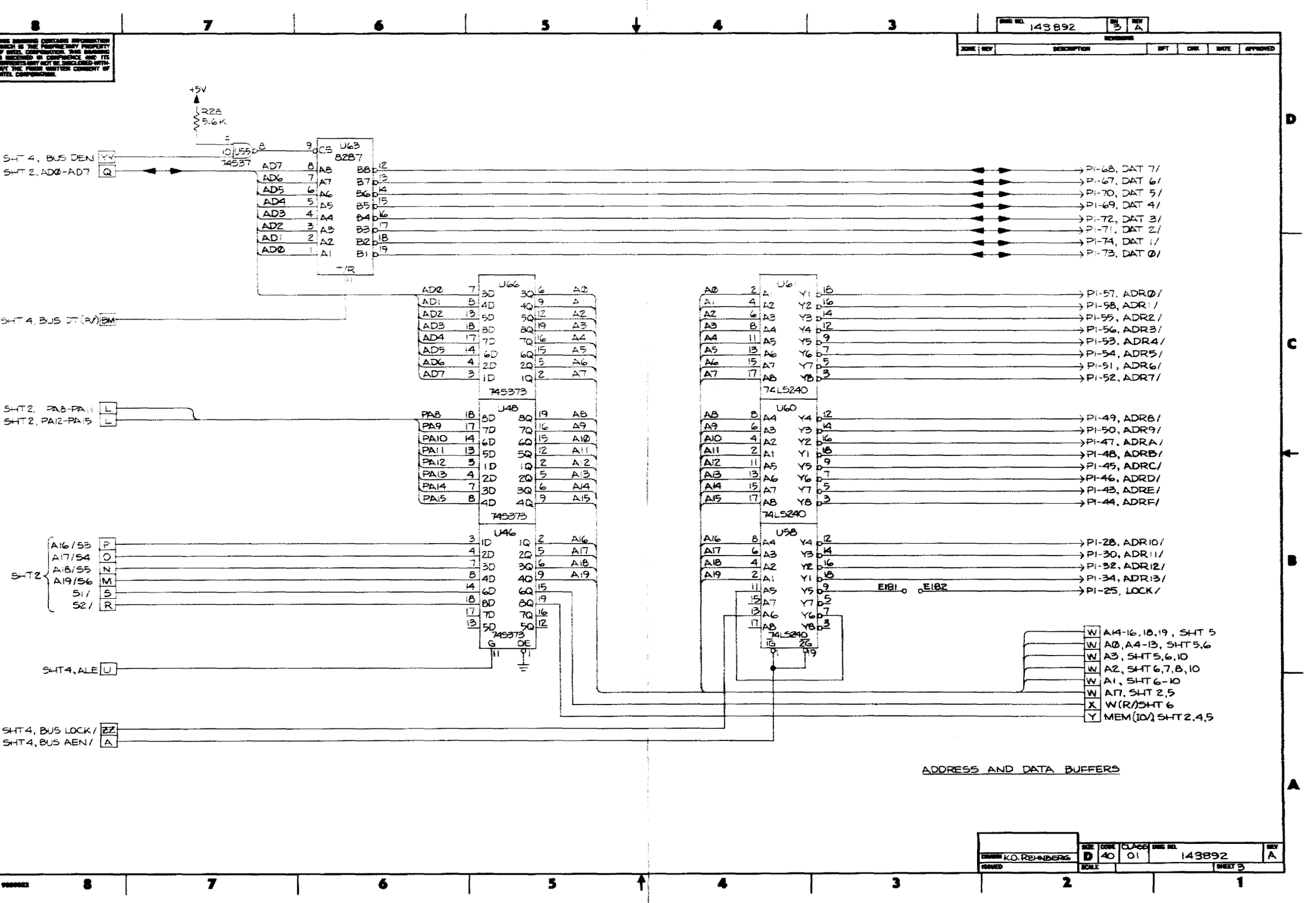
TITLE: SCHEMATIC, iSBC 88/25

SIZE	DOC. CLASS	DOC. CODE	RELEASE LEVEL	DOCUMENT NUMBER	REV
D	40	01		143892	A

SCALE NONE SHEET 1 OF 10

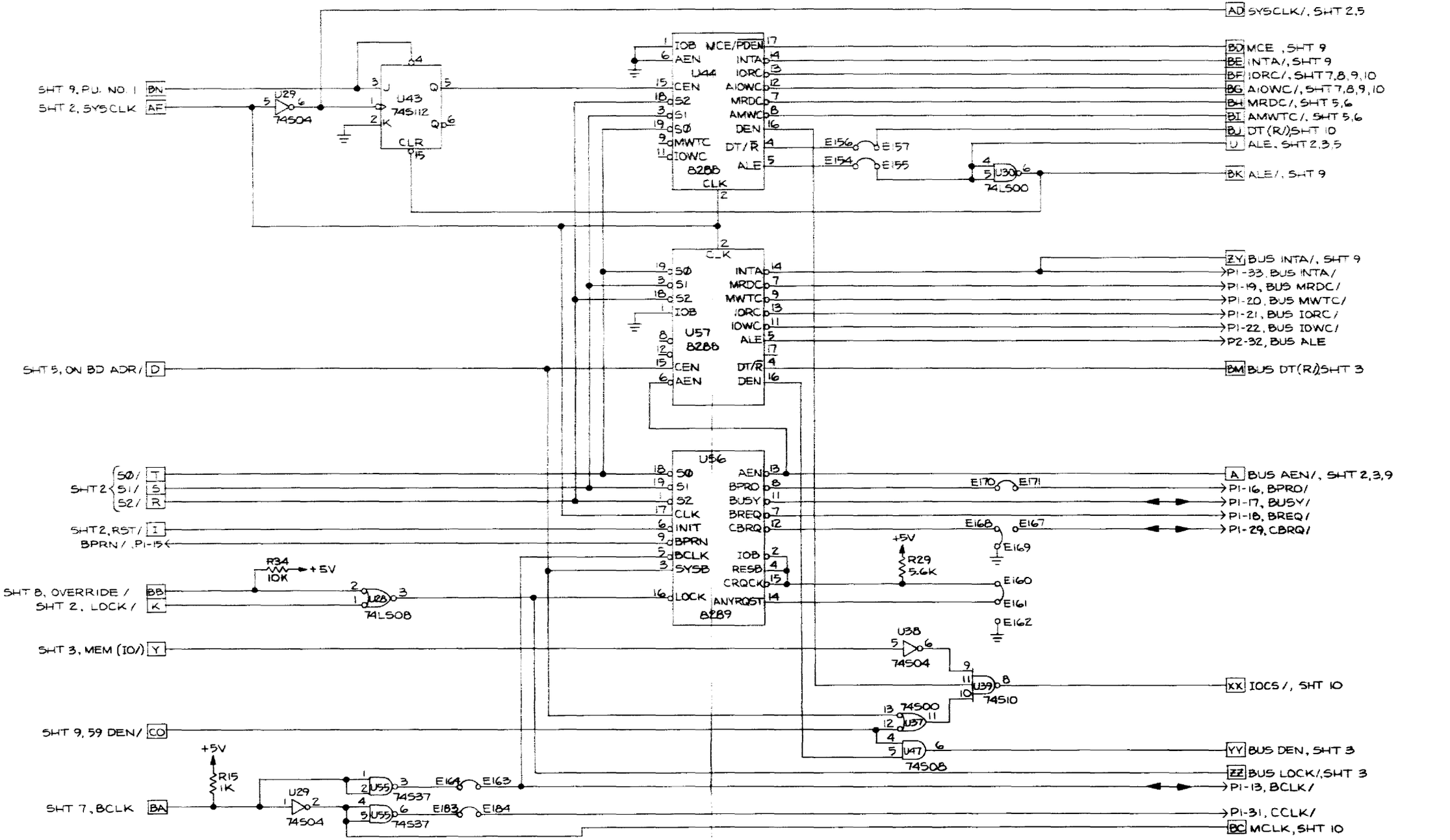
8 7 6 5 4 3 2 1


SHT 9, INTA LOCK
SHT 9, 59 INTA/
SHT 4, ALE
SHT 4, SYS CLK/
SHT 9, PU NO. 2
3 WAIT/
2 WAIT/
1 WAIT/
Ø WAIT/
PROM SYNC RDY
SHT 9, LOCAL INTA
I/O SYNC RDY
I/O ACCESS
I/O ASYNC RDY
SHT 3, MEM (IO)/
SHT 3, A17
MEM RDY
SHT 6, BUSY/
SHT 6, RDY/
PROM ASYNC RDY
SHT 10, MWAIT 2/
SHT 10, MWAIT 1/
ACKNOWLEDGE TIMEOUT
ON BOARD RDY
P1-23, XACK
P2-38, AUX RESET/
SHT 4, BUS AEN/
SHT 5, ON BD ADR/
SHT 9, INTA LOCK/
P1-14, INIT /
P2-36, BD RESET/
SHT 8, TEST/
SHT 9, INTR
SHT 9, NMI
RST/, SHT 4,9
RST, SHT 7,8,10
SYS CLK, SHT 4
LOCK/, SHT 4
A19/S6
A18/S5
A17/S4
A16/S3
SHT 3
PA12-PA15, SHT 3
PA8-PA11, SHT 9,3
AD0-AD7, SHT 3,6,10
S2/, SHT 3,4
S1/, SHT 3,4
S0/, SHT 4
PROCESSOR SECTION
U5 74LS123
U45 8284A
U32 8088
U17 8224
U4 74S175
74LS08
74S02
74S00
74S10
74S04
74LS00
7406
R1 10K
R2 220K
R10 100K
R21 10K
R22 10K
R23 10K
R24 510
R25 100K
R26 560
R32 510
R33 510
R20 510
CR1 IN4148
CR2 IN4148
C12 10±20% 15V
C46 10±20% 15V
C54 0.1
C55 0.1
Y2 12.500 MHz
Y3 15MHz
K.O. REHMBERG
D
40
01
143892
A
SHEET 2


DWG NO. 143892
REV A
+5V
R28
5.6K
U55D
74S37
U63
8287
SHT 4, BUS DEN YY
SHT 2, AD0-AD7 Q
AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0
A8 A7 A6 A5 A4 A3 A2 A1
B8 B7 B6 B5 B4 B3 B2 B1
T/R
PI-68, DAT 7/
PI-67, DAT 6/
PI-70, DAT 5/
PI-69, DAT 4/
PI-72, DAT 3/
PI-71, DAT 2/
PI-74, DAT 1/
PI-73, DAT 0/
SHT 4, BUS DT(R/) BM
U66
U6
74LS373
74LS240
PI-57, ADR0/
PI-58, ADR1/
PI-55, ADR2/
PI-56, ADR3/
PI-53, ADR4/
PI-54, ADR5/
PI-51, ADR6/
PI-52, ADR7/
SHT2, PA8-PA11 L
SHT2, PA12-PA15 L
U48
U60
PI-49, ADR8/
PI-50, ADR9/
PI-47, ADRA/
PI-48, ADRB/
PI-45, ADRC/
PI-46, ADRD/
PI-43, ADRE/
PI-44, ADRF/
SHT2 A16/S3 P
A17/S4 O
A18/S5 N
A19/S6 M
S1/ S
S2/ R
U46
U58
PI-28, ADR10/
PI-30, ADR11/
PI-32, ADR12/
PI-34, ADR13/
PI-25, LOCK/
E181
E182
SHT4, ALE U
W A14-16, 18, 19, SHT 5
W A0, A4-13, SHT 5, 6
W A3, SHT 5, 6, 10
W A2, SHT 6, 7, 8, 10
W A1, SHT 6-10
W A17, SHT 2, 5
X W(R/)SHT 6
Y MEM(IO/) SHT 2, 4, 5
SHT4, BUS LOCK/ ZZ
SHT4, BUS AEN/ A
ADDRESS AND DATA BUFFERS
DRAWN K.O. REHNBERG
ISSUED
SIZE D
CODE 40
CLASS 01
DWG NO. 143892
REV A
SCALE
SHEET 3

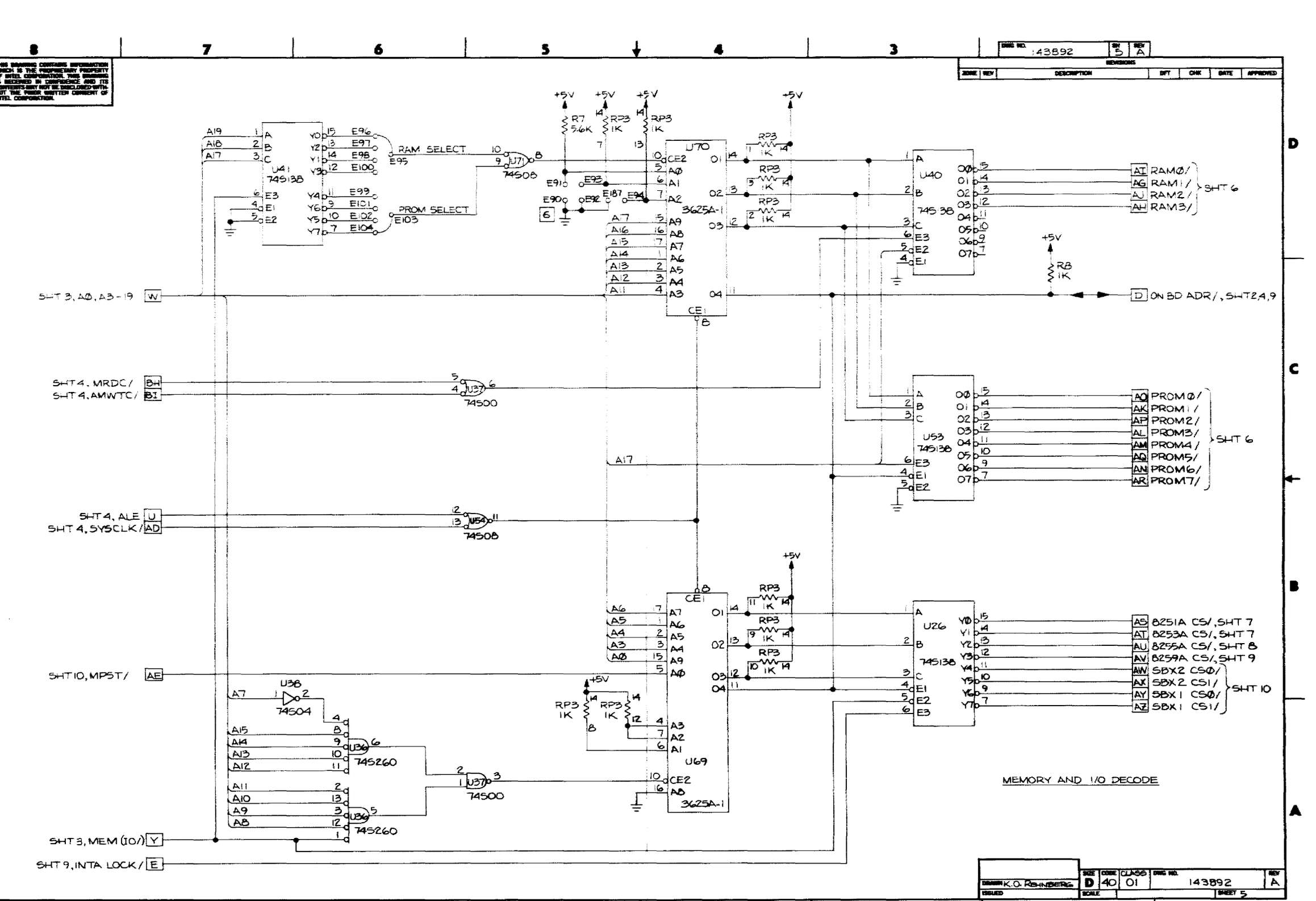
REVISIONS

ZONE	REV	DESCRIPTION	SHT	CHK	DATE	APPROVED



MULTIBUS INTERFACE

DRAWN K.O. REHNBERG	SIZE D	CODE 40	CLASS 01	DWG NO. 143892	REV A
ISSUED	SCALE			SHEET 4	


DRWG NO. 143892 SH 5 REV A
REVISIONS
ZONE REV DESCRIPTION DFT CHK DATE APPROVED
U41 74S138
RAM SELECT
PROM SELECT
U71 74S08
U70 3625A-1
U40 74S138
U53 74S138
U54 74S08
U37 74S00
U38 74S04
U36 74S260
U69 3625A-1
U26 74S138
RAM0/ RAM1/ RAM2/ RAM3/ SHT 6
PROM0/ PROM1/ PROM2/ PROM3/ PROM4/ PROM5/ PROM6/ PROM7/ SHT 6
8251A CS/, SHT 7
8253A CS/, SHT 7
8255A CS/, SHT 8
8259A CS/, SHT 9
SBX2 CS0/
SBX2 CS1/
SBX1 CS0/
SBX1 CS1/
SHT 10
SHT 3, A0, A3-19
ON BD ADR/, SHT 2,4,9
SHT 4, MRDC/
SHT 4, AMWTC/
SHT 4, ALE
SHT 4, SYSCLK/
SHT 10, MPST/
SHT 3, MEM (IO/)
SHT 9, INTA LOCK/
MEMORY AND I/O DECODE
DRAWN K.O. REINBERG
ISSUED
SIZE D CODE 40 CLASS 01 DRG NO. 143892 REV A
SCALE
SHEET 5

DWG NO. 143892 SH 6 REV A

REVISIONS

ZONE	REV	DESCRIPTION	EFT	CHK	DATE	APPROVED

SHT2, AD0-AD7 Q
SHT 3, A0-A13 W
MPRO/, P2-20
SHT 3, W(R)/ X

+5V
E146 HIGH
E145
E143 A11
E144 LOW

+5VB
R19 10K

U49 74LS00

U67 2168R
U51 2168R
U68 9 2168R
U52 9 2168R

RAM

AD0 J8-6
AD1 J8-7
AD2 J8-8
AD3 J8-9
AD4 J8-2
AD5 J8-3
AD6 J8-4
AD7 J8-5
J8-10
J8-1

LSBC 302
RAM EXPANSION

SHT5 RAM0/ AI
RAM1/ AG
RAM2/ AJ
RAM3/ AH

SHT4, MRDC / BH

U33 9
U64 9
U34 9
U65 9

ROM / PROM

+5V
VCC 28
GND 14

SHT5 PROM0/ AO
PROM1/ AK
PROM2/ AP
PROM3/ AL

R18 10K
R12 10K
E141
E142

SHT5 PROM4/ AM
PROM5/ AQ
PROM6/ AN
PROM7/ AR
SHT4, AMWTC/ BI
Vpp, P2-6

NC J7-8
J7-6
J7-4
J7-7
J7-5
J7-2
J7-1
J7-3

C35 6.8 35V 20%

LSBC 341
PROM EXPANSION

6 J6

U6 74LS04
BU BUSY/, SHT2
BV RDY/, SHT2

RP1

MEMORY

DRAWN K.O. REHNBERG	SIZE D	CODE 40	CLASS 01	DWG NO. 143892	REV A
ISSUED	SCALE			SHEET 6	

DWG NO. 143892 SH 7 REV A

ZONE	REV	DESCRIPTION	BY	CHK	DATE	APPROVED

USART DATA I/O: D8h
USART MODE / I/O: DAh
STATUS

SHT 3, A1-A2 W
SHT 5, 8251A CS/ AS
SHT 10, D0-D7 Z
SHT 2, RST J
REQUEST TO SEND, J2-8
TRANSMIT DATA, J2-4
DATA TERM RDY, J2-13
EXTERNAL CLOCK, J2-7
SHT 4, AIOWC/ BG
SHT 4, IORC/ BF
SHT 8, EXT CLK/ BX
PLC, P2-31
SHT 5, 8253A CS/ AT
SHT 8 { GATE 0 CNTRL BY, GATE 1 CNTRL BZ, STXD CA }

U24 8251A
D0 27, D1 28, D2 1, D3 2, D4 5, D5 6, D6 7, D7 8
CS 11, C/D 12, RESET 21, RD 13, WR 10
CTS/ 17, RXD 3, DSR 22, CLK 20, TXC 9, RXC 25
RTS 23, TXD 19, DTR 24, TXRDY 15, RXRDY 14, SYNDET/BD 16, TxEMPTY 18

U14 75188 (x3)
→ J2-10, CLEAR TO SEND
→ J2-6, RECEIVE DATA
→ J2-12, DATA SET RDY

U15 75189 (x4)
E88, E89

CB SITX INTR, SHT 9
CC SIRX INTR, SHT 9

E76, E77, E78, E79, E80, E81

E69, E70, E71, E73
U14 75188
→ E72 J2-26, SEC. CLEAR TO SEND
→ E75 J2-5, SEC. RECEIVE DATA
→ E74 J2-21, TRANSMIT SIG. ELEMENT TIMING

BA BCLK, SHT 4

U16 8224 TANK
VDD, OSC, RDYIN, READY, RESIN, RESET, SYNC, Φ1, Φ2, OSCTTL, XTAL2, XTAL1
Y1 19.6608MHz
R30 510, R31 510
E86, E87

U12 74S163
CLK, CLR, ENP, ENT, LOAD, QA, QB, QC, QD, CY
R6 1K

U13 74S163
ENP, ENT, CLR, LOAD, CLK, A, B, C, D, QA, QB, QC, QD, CY

E62, E60, E64, E61, E55, E56, E57, E58, E54, E59, E63

U23 8253-5
D0 8, D1 7, D2 6, D3 5, D4 4, D5 3, D6 2, D7 1
RD 22, WR 23
CLK0 9, CLK1 15, CLK2 18
OUT2 17, OUT0 10, OUT1 13
A0 19, A1 20
GATE2 16, CS 21
GATE0 11, GATE1 14
R13 10K

CE TIMER 0 INTR, SHT 9
CF TIMER 1 INTR, SHT 9

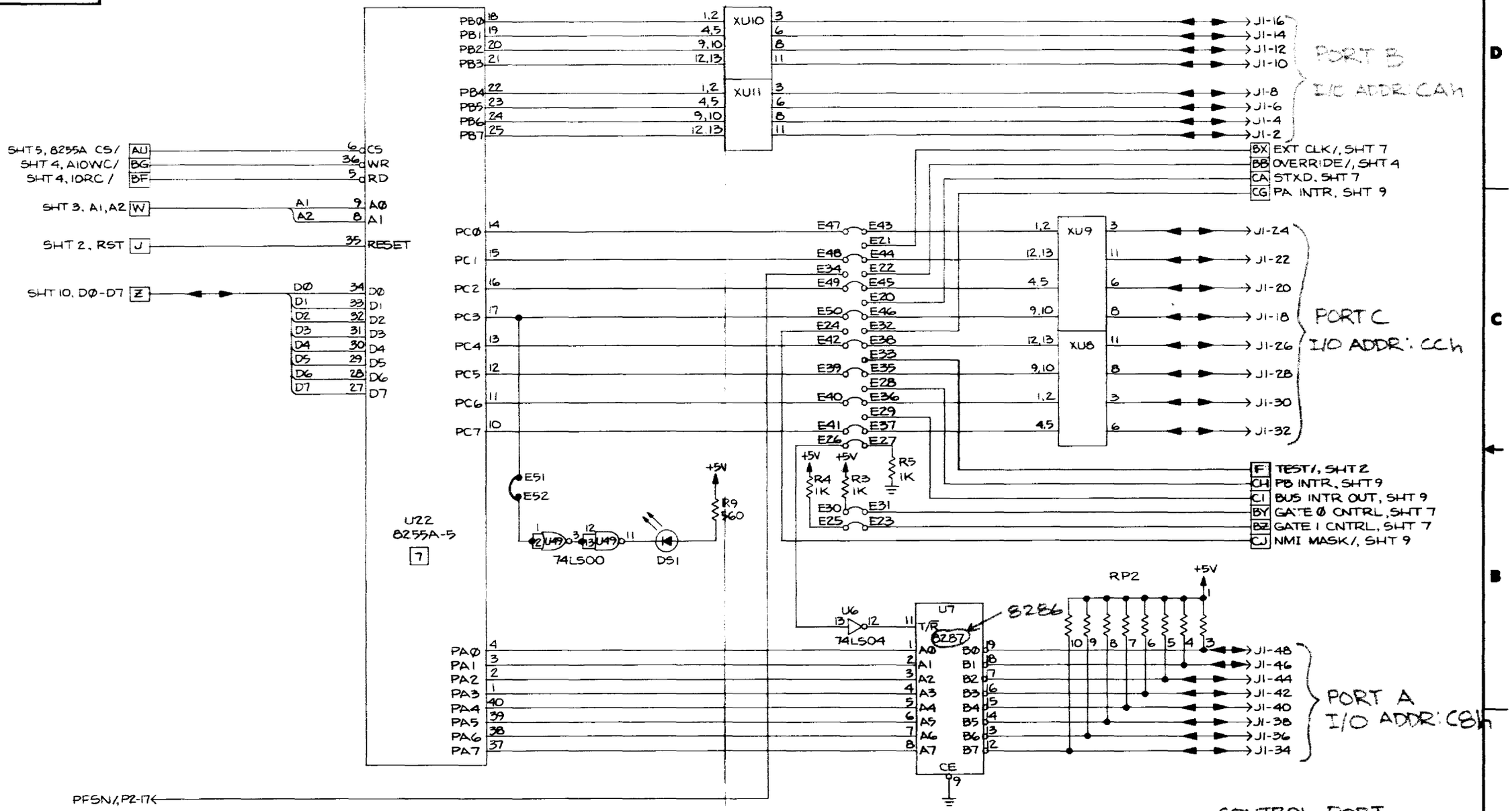
CNTR 0 I/O: D0h
CNTR 1 I/O: D2h
CNTR 2 I/O: D4h
CONTROL I/O: D6h

S6 PLC, SHT 9

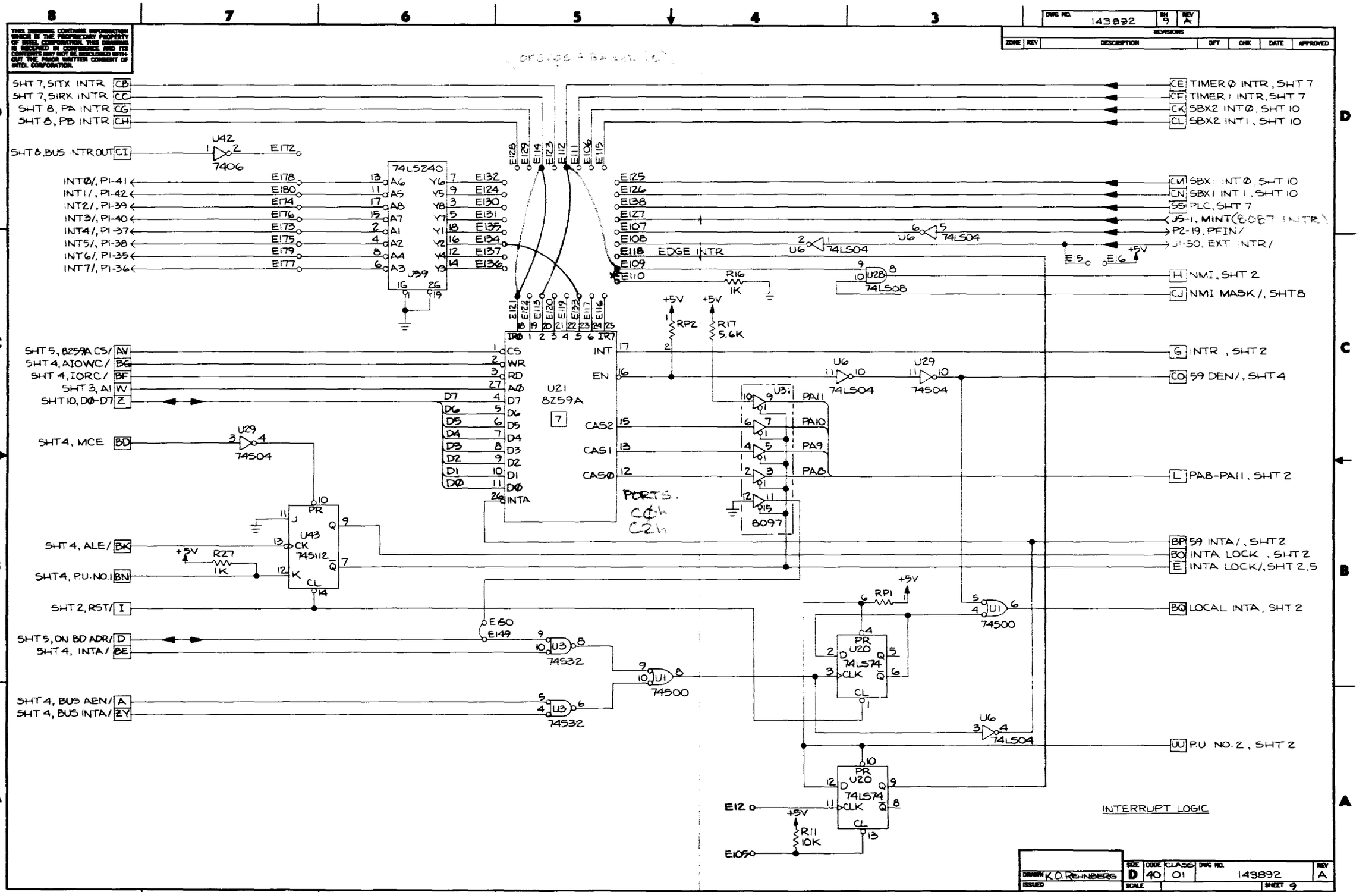
TIMER AND SERIAL PORTS

DRAWN	SIZE	CODE	CLASS	DWG NO.	REV
K.O. REINBERG	D	40	01	143892	A

ZONE	REV	DESCRIPTION	DFT	CHK	DATE	APPROVED



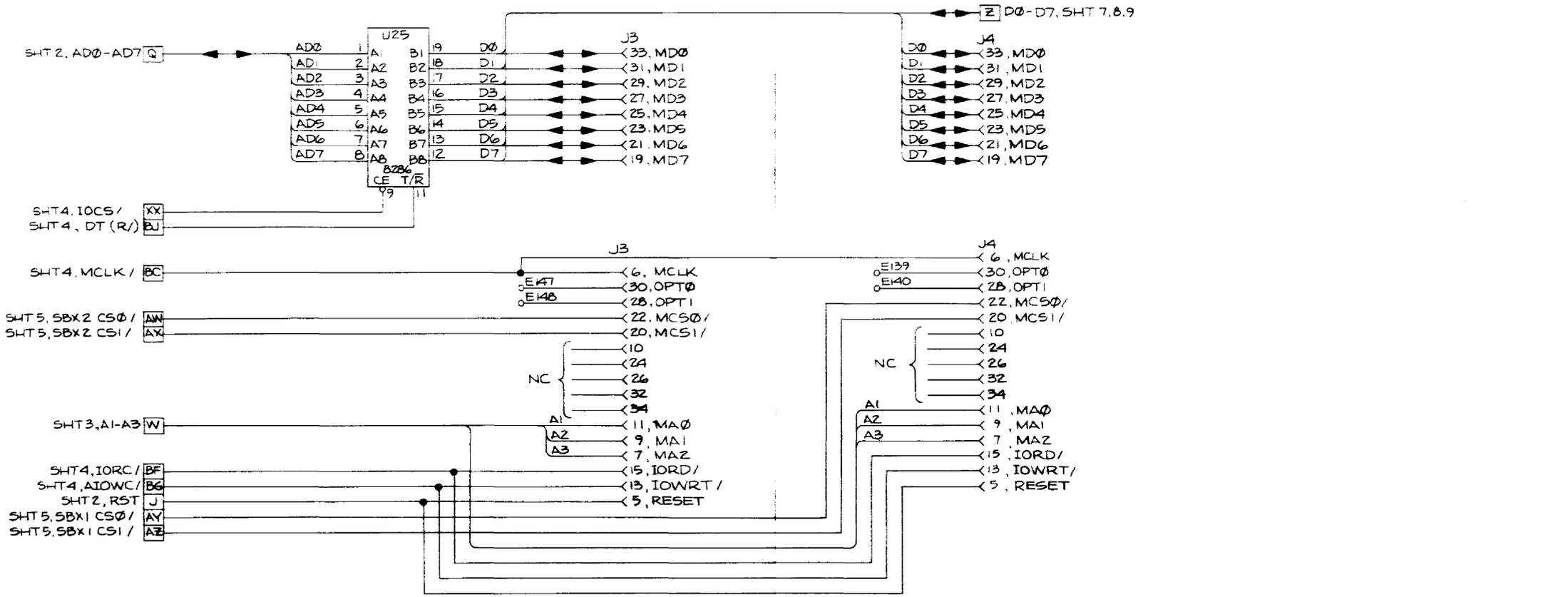
DRAWN	SIZE	CODE	CLASS	DWG NO.	REV
K.O.REHNBERG	D	40	01	143892	A
ISSUED	SCALE			SHEET 6	


8
7
6
5
4
3
DWG NO. 143892
SH 9
REV A
REVISIONS
ZONE REV DESCRIPTION DFT CHK DATE APPROVED
THIS DRAWING CONTAINS INFORMATION WHICH IS THE PROPRIETARY PROPERTY OF INTEL CORPORATION. THIS DRAWING IS RECEIVED IN CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED WITHOUT THE PRIOR WRITTEN CONSENT OF INTEL CORPORATION.
SHT 7, SITX INTR CB
SHT 7, SIRX INTR CC
SHT 8, PA INTR CG
SHT 8, PB INTR CH
SHT 8, BUS INTR OUT CI
U42
7406
E172
74LS240
INTØ/, PI-41
INT1/, PI-42
INT2/, PI-39
INT3/, PI-40
INT4/, PI-37
INT5/, PI-38
INT6/, PI-35
INT7/, PI-36
E178
E180
E174
E176
E173
E175
E179
E177
U59
E132
E124
E130
E131
E135
E134
E137
E136
E128
E129
E114
E123
E112
E111
E106
E115
E125
E126
E138
E127
E107
E108
E118 EDGE INTR
E109
E110
R16 1K
E121
E122
E113
E120
E119
E133
E117
E116
+5V
RPZ
R17 5.6K
U21 8Z59A
7
IR0 1 2 3 4 5 6 IR7
CS
WR
RD
AØ
D7
D6
D5
D4
D3
D2
D1
DØ
INTA
INT
EN
CAS2
CAS1
CASØ
SHT 5, 8259A CS/ AV
SHT 4, AIOWC/ BG
SHT 4, IORC/ BF
SHT 3, AI W
SHT 10, DØ-D7 Z
SHT 4, MCE BD
U29
74504
SHT 4, ALE/ BK
SHT 4, P.U. NO.1 BN
SHT 2, RST/ I
R27 1K
U43
74S112
PR
CK
CL
J
K
Q
SHT 5, ON BD ADR/ D
SHT 4, INTA/ BE
E150
E149
U3
74S32
SHT 4, BUS AEN/ A
SHT 4, BUS INTA/ ZY
U1
74S00
U31
8097
PA11
PA10
PA9
PA8
PORTS C0h C2h
U6
74LS04
U28
74LS08
E15
E16
+5V
CE TIMER Ø INTR, SHT 7
CF TIMER 1 INTR, SHT 7
CK SBX2 INTØ, SHT 10
CL SBX2 INT1, SHT 10
CM SBX1 INTØ, SHT 10
CN SBX1 INT 1, SHT 10
55 PLC, SHT 7
J5-1, MINT (8087 INTR)
P2-19, PFIN/
J1-50, EXT INTR/
H NMI, SHT 2
CJ NMI MASK/, SHT 8
G INTR, SHT 2
CO 59 DEN/, SHT 4
L PA8-PA11, SHT 2
BP 59 INTA/, SHT 2
BO INTA LOCK, SHT 2
E INTA LOCK/, SHT 2,5
BQ LOCAL INTA, SHT 2
UU P.U NO. 2, SHT 2
RP1
U20
74LS74
D
CLK
Q
E12
E105
R11 10K
INTERRUPT LOGIC
DRAWN K.O. RENNBERG
ISSUED
SIZE D
CODE 40
CLASS 01
DWG NO. 143892
REV A
SCALE
SHEET 9

DWG NO. 143892 SH 1/0 REV A

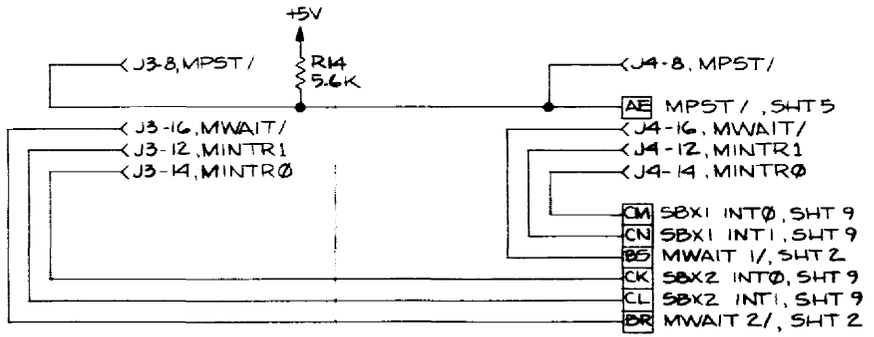
REVISIONS

ZONE	REV	DESCRIPTION	DFT	CHK	DATE	APPROVED



J3	
PORT NO.	SELECT
80, 82, 84, 86, 88, 8A, 8C, 8E	MCS0
90, 92, 94, 96, 98, 9A, 9C, 9E	MCS1

J4	
PORT NO.	SELECT
A0, A2, A4, A6, A8, AA, AC, AE	MCS0
B0, B2, B4, B6, B8, BA, BC, BE	MCS1



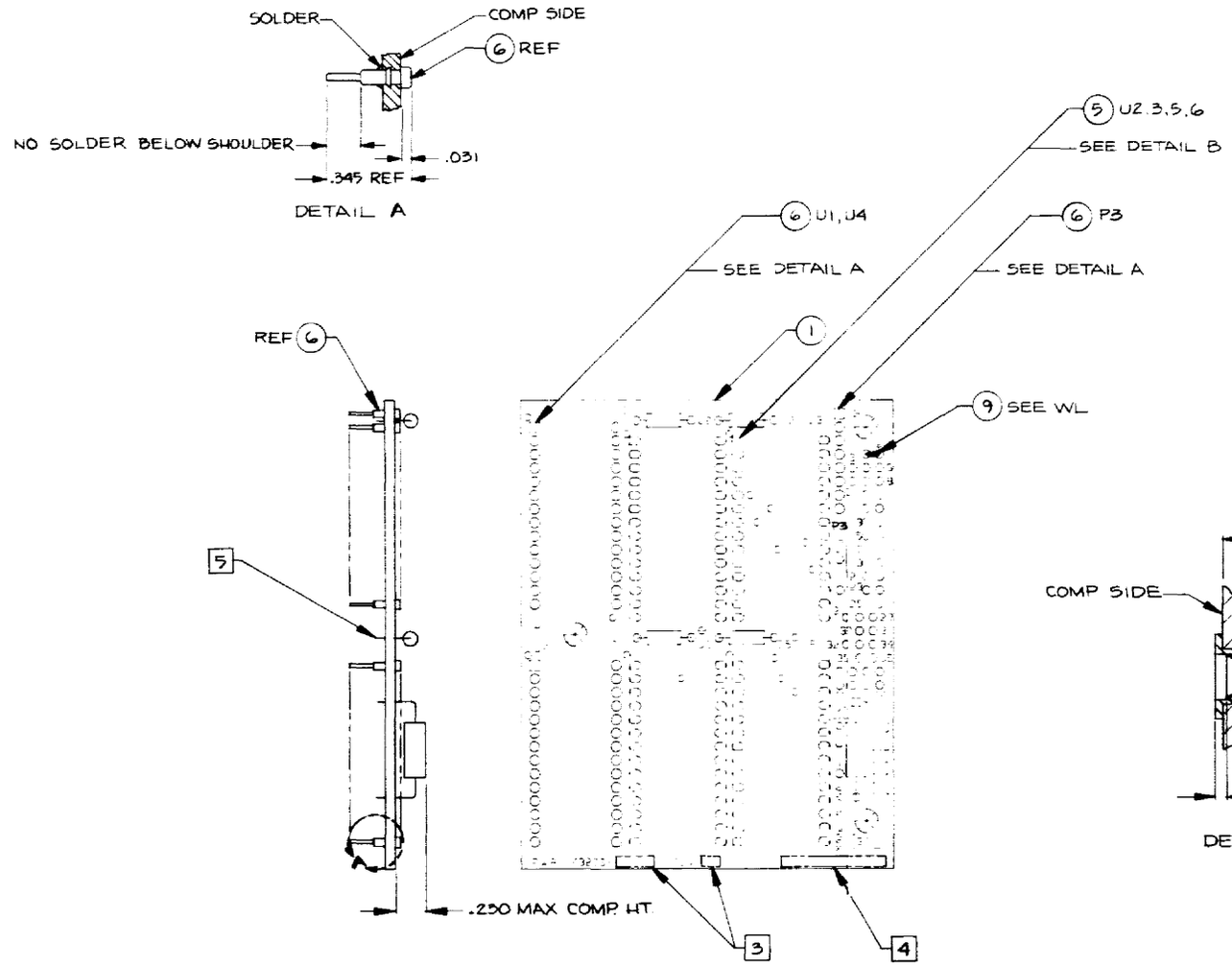
iSBX CONNECTORS

DRAWN K.O. KEHNBERG
ISSUED
SIZE D CODE 40 CLASS 01 DWG NO. 143892 REV A
SCALE
SHEET 10

DWG NO. 143279 SH 1 REV A

REVISIONS

ZONE	REV	DESCRIPTION	BY	CHK	DATE
	A	ECO 40-2405	[illegible]	[illegible]	2/6/81



NOTES: UNLESS OTHERWISE SPECIFIED

1. ASSEMBLY PART NUMBER IS 143279-001. THIS DOCUMENT, PL AND WL ARE TRACKING DOCUMENTS.
2. WORKMANSHIP PER 99-0007-001.
3. MARK ASSEMBLY DASH NUMBER AND REVISION LEVEL WITH CONTRASTING PERM. COLOR, NON-CONDUCTIVE, .12 HIGH, APPROXIMATELY WHERE SHOWN.
4. MARK ASSEMBLY VENDOR I.D. WITH CONTRASTING PERM. COLOR, NON-CONDUCTIVE, .12 HIGH, APPROXIMATELY WHERE SHOWN.
5. TRIM COMPONENT LEADS AFTER ASSY TO .05 MAX.
6. ALL I.C.S, U1-U6, ARE SUPPLIED BY CUSTOMER.

QUANTITY PER DASH NO.

UNLESS OTHERWISE SPECIFIED:
1. DIMENSIONS ARE IN INCHES.
2. BREAK ALL SHARP EDGES.
3. DO NOT SCALE DRAWING.
4. TOLERANCES: ANGLES ± 2° XX ± .030 XXX ± .010
SURFACE FINISH √

NEXT ASSY | USED ON

ITEM NO. | PART NUMBER | DESCRIPTION

PARTS LIST

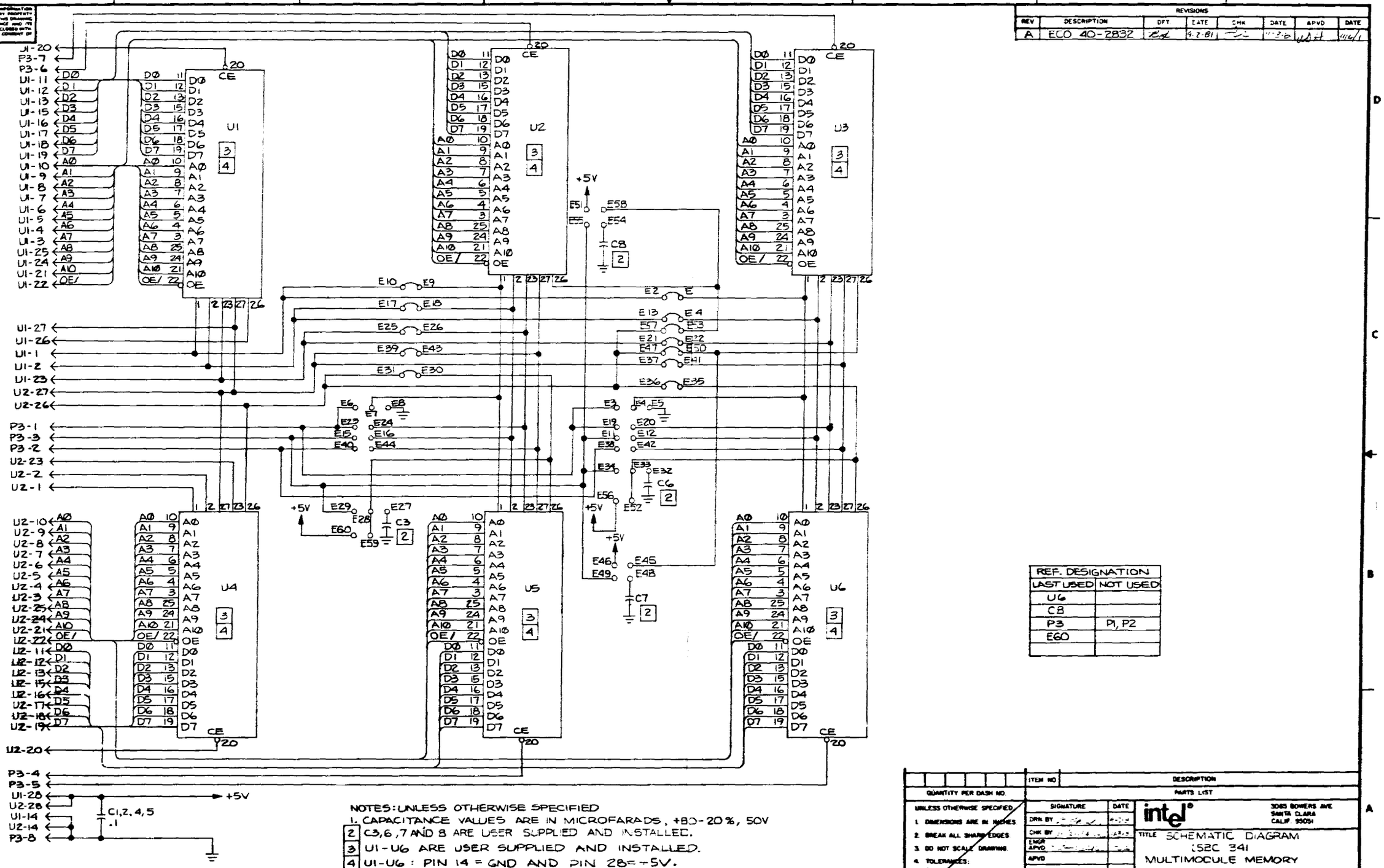
SIGNATURE	DATE
DRN BY KORENBERG	1/30/81
CHK BY J. BUCHANAN	2/4/81
APVD [illegible]	2/6/81
APVD	
APVD	

intel® 3065 BOWERS AVE. SANTA CLARA CALIF. 95051

TITLE
PRINTED WIRING ASSEMB
MEMORY EXPANSION
iSBC 341

SIZE	CODE	CLASS	DWG NO.
D	40	05	143279

SCALE 2:1 SHEET



REVISIONS							
REV	DESCRIPTION	DFT	DATE	CHK	DATE	APVD	DATE
A	ECO 40-2832		9-2-81				

REF. DESIGNATION	
LAST USED	NOT USED
U6	
C8	
P3	P1, P2
E60	

ITEM NO	DESCRIPTION
	PARTS LIST

QUANTITY PER DASH NO.

UNLESS OTHERWISE SPECIFIED
1. DIMENSIONS ARE IN INCHES
2. BREAK ALL SHARP EDGES
3. DO NOT SCALE DRAWING
4. TOLERANCES: ANGLES ±, X.X ±, XXX ±

SIGNATURE	DATE
DRN BY	
CHK BY	
ENGR APVD	
APVD	
APVD	

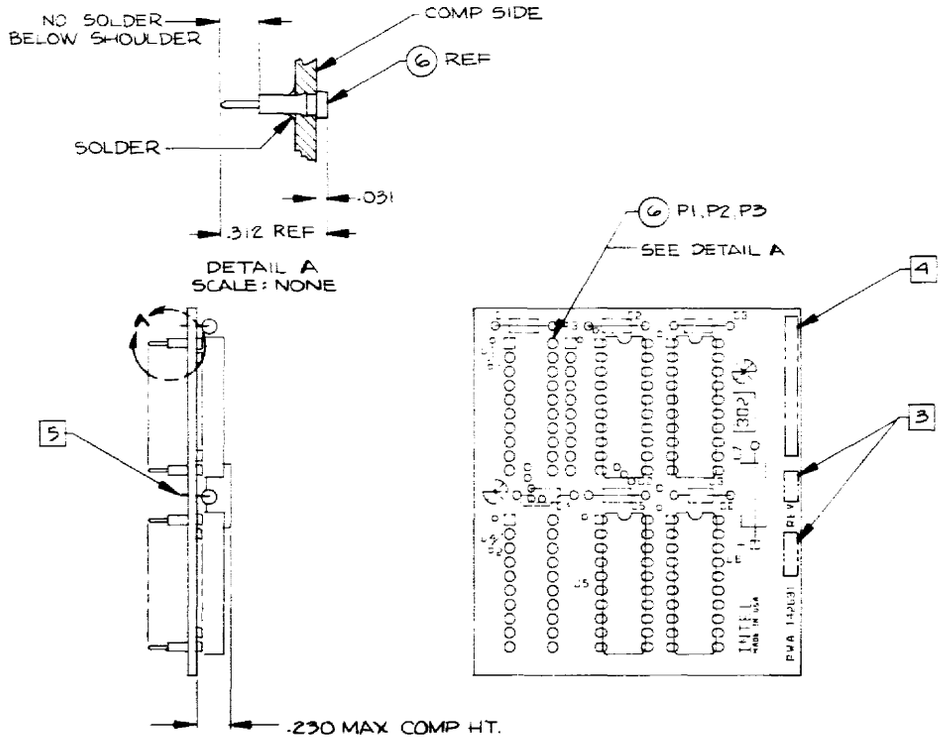
intel
3065 BOWERS AVE
SANTA CLARA
CALIF. 95051

TITLE SCHEMATIC DIAGRAM
iSBC 341
MULTIMODULE MEMORY

SIZE	DCLC	CL CODE	RLSE LVL	DOCUMENT NUMBER	REV
D	40	01		142853	A

SCALE: NONE SHEET OF 1

REVISIONS						
REV	DESCRIPTION	DFT	DATE	CHK	DATE	APVD
A	ECO 40-2419	KR	[illegible]	[illegible]	[illegible]	[illegible]



NOTES: UNLESS OTHERWISE SPECIFIED

1. ASSEMBLY PART NUMBER IS 142961-001. THIS DOCUMENT AND PL ARE TRACKING DOCUMENTS.
2. WORKMANSHIP PER 99-0007-001.
3. MARK ASSEMBLY DASH NUMBER AND REVISION LEVEL WITH CONTRASTING PERM. COLOR, NON-CONDUCTIVE, .12 HIGH, APPROXIMATELY WHERE SHOWN.
4. MARK ASSEMBLY VENDOR I.D. WITH CONTRASTING PERM. COLOR, NON-CONDUCTIVE, .12 HIGH, APPROXIMATELY WHERE SHOWN.
5. TRIM COMPONENT LEADS AFTER ASSY TO .05 MAX.
6. I.C.'S U1 AND U4 ARE SUPPLIED AND INSTALLED BY CUSTOMER.

QUANTITY PER DASH NO.	ITEM NO.	DESCRIPTION
		PARTS LIST

UNLESS OTHERWISE SPECIFIED:
1. DIMENSIONS ARE IN INCHES.
2. BREAK ALL SHARP EDGES.
3. DO NOT SCALE DRAWING.
4. TOLERANCES:
.XX ±
.XXX ±

	SIGNATURE	DATE
DRN BY	KOR	[illegible]
CHK BY	J B[illegible]	[illegible]
ENGR APVD	[illegible]	[illegible]
APVD		
APVD		

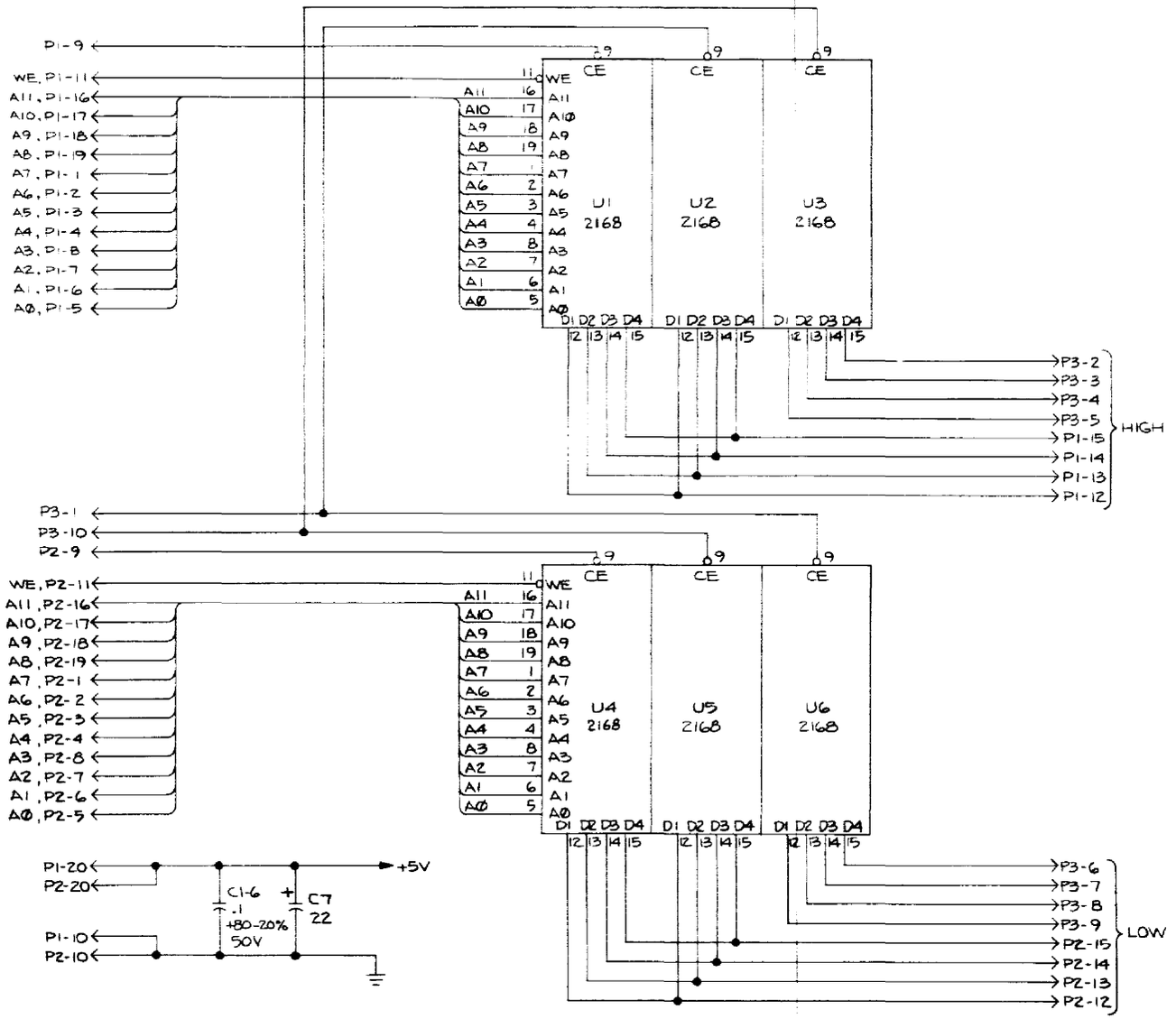
intel
3065 BOWER
SANTA CLA
CALIF. 950

TITLE: PRINTED WIRING ASSY
LSBC 302
MEMORY EXPANSION

SIZE	DCL C	CL CODE	RLSE LVL	DOCUMENT NUMBER
D	40	05		142961

SCALE 2:1 SHEET

REVISIONS							
REV	DESCRIPTION	DFT	DATE	CHK	DATE	APVD	DATE
A	ECO 40-2419	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]



REF. DESIGNATION	
LAST USED	NOT USED
U6	
C7	
P3	

POWER, GROUND AND SPARE GATE LOCATOR				
REF DES	DEVICE TYPE	POWER PINS GND	POWER PINS +5V	SPARE GATES OUTPUT PINS
U1,4	SOCKET	10	20	
U2,3,5,6	2168	10	20	

NOTES: UNLESS OTHERWISE SPECIFIED
CAPACITANCE VALUES ARE IN MICROFARADS, 10%, 15V.

ITEM NO.	DESCRIPTION
QUANTITY PER DASH NO.	PARTS LIST

UNLESS OTHERWISE SPECIFIED:
1. DIMENSIONS ARE IN INCHES.
2. BREAK ALL SHARP EDGES.
3. DO NOT SCALE DRAWING.
4. TOLERANCES: ANGLES ±, XX ±, XXX ±

SIGNATURE	DATE
DRN BY [illegible]	[illegible]
CHK BY J. BUCHANAN	[illegible]
ENGR APVD [illegible]	[illegible]
APVD	
APVD	

intel
3065 BOWERS AVE.
SANTA CLARA
CALIF. 95051

TITLE
SCHEMATIC
iSBC 302

SIZE	DCL C	CL CODE	RLSE LVL	DOCUMENT NUMBER	REV
D	40	01		142963	A

SCALE | SHEET 1 OF 1

APPENDIX A
DECODE PROM MEMORY MAPS

MEMORY DECODE PROM (U70)

The iSBC 88/25 board utilizes one Intel pre-programmed PROM in the memory decode circuitry. Decode PROM operation is discussed in sections 4-7 and 4-8 of the text. Table A-1 is the PROM memory map for the memory decode PROM.

I/O DECODE PROM (U69)

The iSBC 88/25 board utilizes one Intel pre-programmed PROM in the I/O decode circuitry. Decode PROM operation is discussed in sections 4-7 and 4-9 of the text. Table A-2 is the PROM memory map for the I/O decode PROM.

Table A-1. Memory Decode PROM (U70) Map Part No. 144011-001

8000	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
8010	02	02	02	02	0F	0F	0F	0F	02	02	02	02	0F	0F	0F	0F
8020	03	03	03	03	0F	0F	0F	0F	03	03	03	03	0F	0F	0F	0F
8030	01	01	01	01	0F	0F	0F	0F	01	01	01	01	0F	0F	0F	0F
8040	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
8050	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
8060	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
8070	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
8080	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
8090	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
80A0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
80B0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
80C0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
80D0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
80E0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
80F0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
8100	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
8110	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
8120	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
8130	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
8140	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
8150	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
8160	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
8170	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
8180	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
8190	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
81A0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
81B0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
81C0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
81D0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
81E0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
81F0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
8200	07	0F	0F	0F	0F	0F	0F	0F	07	0F	0F	0F	0F	0F	0F	0F
8210	07	0F	0F	0F	0F	0F	0F	0F	07	0F	0F	0F	0F	0F	0F	0F
8220	07	0F	0F	0F	0F	0F	0F	0F	07	0F	0F	0F	0F	0F	0F	0F

(continued)

Table A-1. Memory Decode PROM (U70) Map
Part No. 144011-001
(Continued)

8230	07	0F	0F	0F	0F	0F	0F	0F	07	0F	0F	0F	0F	0F	0F	0F
8240	06	0F	0F	0F	0F	0F	0F	0F	06	0F	0F	0F	0F	0F	0F	0F
8250	06	0F	0F	0F	0F	0F	0F	0F	06	0F	0F	0F	0F	0F	0F	0F
8260	06	0F	0F	0F	0F	0F	0F	0F	06	0F	0F	0F	0F	0F	0F	0F
8270	06	0F	0F	0F	0F	0F	0F	0F	06	0F	0F	0F	0F	0F	0F	0F
8280	05	0F	0F	0F	0F	0F	0F	0F	05	0F	0F	0F	0F	0F	0F	0F
8290	05	0F	0F	0F	0F	0F	0F	0F	05	0F	0F	0F	0F	0F	0F	0F
82A0	05	0F	0F	0F	0F	0F	0F	0F	05	0F	0F	0F	0F	0F	0F	0F
82B0	05	0F	0F	0F	0F	0F	0F	0F	05	0F	0F	0F	0F	0F	0F	0F
82C0	04	0F	0F	0F	0F	0F	0F	0F	04	0F	0F	0F	0F	0F	0F	0F
82D0	04	0F	0F	0F	0F	0F	0F	0F	04	0F	0F	0F	0F	0F	0F	0F
82E0	04	0F	0F	0F	0F	0F	0F	0F	04	0F	0F	0F	0F	0F	0F	0F
82F0	04	0F	0F	0F	0F	0F	0F	0F	04	0F	0F	0F	0F	0F	0F	0F
8300	03	07	0F	0F	03	0F	0F	0F	03	07	0F	0F	03	0F	0F	0F
8310	03	07	0F	0F	03	0F	0F	0F	03	07	0F	0F	03	0F	0F	0F
8320	03	06	0F	0F	03	0F	0F	0F	03	06	0F	0F	03	0F	0F	0F
8330	03	06	0F	0F	03	0F	0F	0F	03	06	0F	0F	03	0F	0F	0F
8340	02	05	0F	0F	02	0F	0F	0F	02	05	0F	0F	02	0F	0F	0F
8350	02	05	0F	0F	02	0F	0F	0F	02	05	0F	0F	02	0F	0F	0F
8360	02	04	0F	0F	02	0F	0F	0F	02	04	0F	0F	02	0F	0F	0F
8370	02	04	0F	0F	02	0F	0F	0F	02	04	0F	0F	02	0F	0F	0F
8380	01	03	07	0F	01	03	0F	0F	01	03	07	0F	01	03	0F	0F
8390	01	03	06	0F	01	03	0F	0F	01	03	06	0F	01	03	0F	0F
83A0	01	02	05	0F	01	02	0F	0F	01	02	05	0F	01	02	0F	0F
83B0	01	02	04	0F	01	02	0F	0F	01	02	04	0F	01	02	0F	0F
83C0	00	01	03	07	00	01	03	0F	00	01	03	06	00	01	03	0F
83D0	00	01	02	05	00	01	02	0F	00	01	02	04	00	01	02	0F
83E0	00	00	01	03	00	00	01	03	00	00	01	02	00	00	01	02
83F0	00	00	00	01	00	00	00	01	00	00	00	00	00	00	00	00

Table A-2. I/O Decode PROM (U69) Map Part No. 143383-001

8000	04	04	0F	0F	0F	0F	04	0F	04	04	0F	0F	0F	0F	04	0F
8010	04	04	0F	0F	0F	0F	04	0F	04	04	0F	0F	0F	0F	04	0F
8020	05	05	0F	0F	0F	0F	05	0F	05	05	0F	0F	0F	0F	05	0F
8030	05	05	0F	0F	0F	0F	05	0F	05	05	0F	0F	0F	0F	05	0F
8040	06	0F	06	0F	0F	0F	06	0F	06	0F	06	0F	0F	0F	06	0F
8050	06	0F	06	0F	0F	0F	06	0F	06	0F	06	0F	0F	0F	06	0F
8060	07	0F	07	0F	0F	0F	07	0F	07	0F	07	0F	0F	0F	07	0F
8070	07	0F	07	0F	0F	0F	07	0F	07	0F	07	0F	0F	0F	07	0F
8080	03	03	03	03	0F	0F	03	03	03	03	03	03	0F	0F	03	03
8090	02	02	02	02	0F	0F	02	02	02	02	02	02	0F	0F	02	02
80A0	01	01	01	01	0F	0F	01	01	01	01	01	01	0F	0F	01	01
80B0	00	00	00	00	0F	0F	00	00	00	00	00	00	0F	0F	00	00
80C0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
80D0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
80E0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
80F0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
8100	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
8110	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
8120	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
8130	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
8140	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
8150	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
8160	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
8170	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
8180	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
8190	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
81A0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
81B0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
81C0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
81D0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
81E0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
81F0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
8200	0F	0F	0F	0F	0F	0F	0F	0F	04	04	0F	0F	0F	0F	04	0F
8210	0F	0F	0F	0F	0F	0F	0F	0F	04	04	0F	0F	0F	0F	04	0F
8220	0F	0F	0F	0F	0F	0F	0F	0F	05	05	0F	0F	0F	0F	05	0F
8230	0F	0F	0F	0F	0F	0F	0F	0F	05	05	0F	0F	0F	0F	05	0F
8240	0F	0F	0F	0F	0F	0F	0F	0F	06	0F	06	0F	0F	0F	06	0F
8250	0F	0F	0F	0F	0F	0F	0F	0F	06	0F	06	0F	0F	0F	06	0F
8260	0F	0F	0F	0F	0F	0F	0F	0F	07	0F	07	0F	0F	0F	07	0F
8270	0F	0F	0F	0F	0F	0F	0F	0F	07	0F	07	0F	0F	0F	07	0F
8280	0F	0F	0F	0F	0F	0F	0F	0F	03	03	03	03	0F	0F	03	03
8290	0F	0F	0F	0F	0F	0F	0F	0F	02	02	02	02	0F	0F	02	02
82A0	0F	0F	0F	0F	0F	0F	0F	0F	01	01	01	01	0F	0F	01	01
82B0	0F	0F	0F	0F	0F	0F	0F	0F	00	00	00	00	0F	0F	00	00
82C0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
82D0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
82E0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
82F0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
8300	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F

(continued)

Table A-2. I/O Decode PROM (U69) Map
Part No. 143383-001
(Continued)

8310	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
8320	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
8330	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
8340	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
8350	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
8360	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
8370	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
8380	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
8390	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
83A0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
83B0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
83C0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
83D0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
83E0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
83F0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F