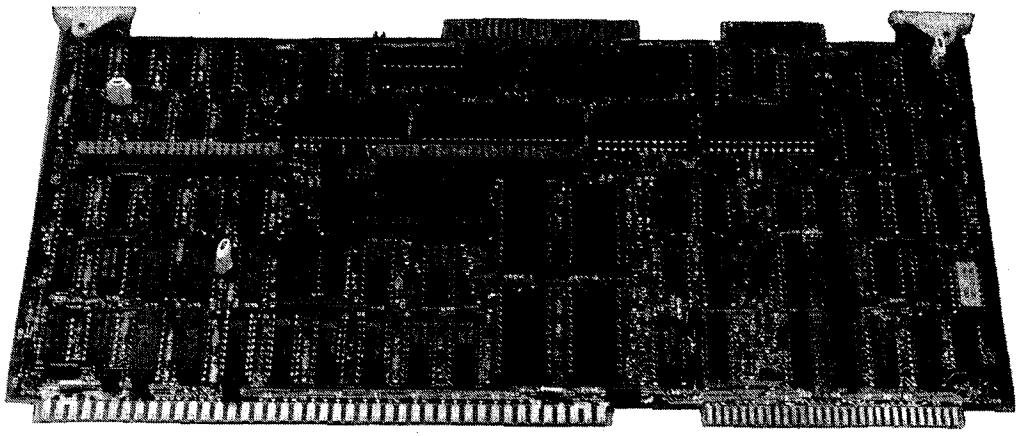
iSBC® 86/05A
SINGLE BOARD COMPUTER

- 8086/10 (8086-2) Microprocessor with 5 or 8 MHz CPU Clock
- Software Compatible with 8086, 8088, 80186, 80286 Based 16-bit Single Board Computers
- Optional 8086/20 Numeric Data Processor with iSBC® 337 A MULTIMODULE™ Processor
- 8K bytes of Static RAM; Expandable On-Board to 16K Bytes
- Sockets for up to 256K Bytes of JEDEC 24/28-Pin Standard Memory Devices; Expandable On-Board to 512K Bytes
- Two iSBX™ Bus Connectors
- Programmable Synchronous/ Asynchronous RS232C Compatible Serial Interface with Software Selectable Baud Rate
- 24 Programmable Parallel I/O Lines
- Two Programmable 16-Bit BCD or Binary Timers/Event Counters
- 9 Levels of Vectored Interrupt Control, Expandable to 65 Levels
- MULTIBUS® Bus Interface for Multimaster Configurations and System Expansion
- Supported by a Complete Family of Single Board Computers, Memory, Digital and Analog I/O, Peripheral Controllers, Packaging and Software

The iSBC 86/05A Single Board Computer is a member of Intel's complete line of OEM microcomputer systems which take full advantage of Intel's technology to provide economical, self-contained, computer-based solutions for OEM applications. The iSBC 86/05A board is a complete computer system on a single 6.75 x 12.00 in. printed circuit card. The CPU, system clock, read/write memory, nonvolatile read only memory, I/O ports and drivers, serial communications interface, priority interrupt logic and programmable timers, all reside on the board. The large control storage capacity makes the iSBC 86/05A board ideally suited for control-oriented applications such as process control, instrumentation, industrial automation, and many others.



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FUNCTIONAL DESCRIPTION

Central Processing Unit

The central processor for the iSBC 86/05A board is Intel's iAPX 86/10 (8086-2) CPU. a clock rate of 8 MHz is supported with a jumper selectable option of 5 MHz. The CPU architecture includes four 16-bit byte addressable data registers, two 16-bit memory base pointer registers and two 16-bit index registers. All are accessed by a total of 24 operand addressing modes for comprehensive memory addressing and for support of the data structures required for today's structured, high level languages as well as assembly language.

Instruction Set

The 8086 instruction repertoire includes variable length instruction format (including double operand instructions), 8- and 16-bit signed and unsigned arithmetic operators for binary, BCD and unpacked ASCII data, and iterative word and byte string manipulation functions.

For enhanced numerics processing capability, the iSBC 337A MULTIMODULE Numeric Data Processor extends the iAPX 86/10 architecture and data set. Over 60 numeric instructions offer arithmetic, trigonometric, transcendental, logarithmic and exponential instructions. Supported data types include 16-, 32-, and 64-bit integer, and 32- and 64-bit floating point, 18-digit packed BCD and 80-bit temporary.

Architectural Features

A 6-byte instruction queue provides pre-fetching of sequential instructions and can reduce the 740 ns minimum instruction cycle to 250 ns for queued instructions. The stack-oriented architecture readily supports modular programming by facilitating fast, simple, inter-module communication, and other programming constructs needed for asynchronous real-time systems. The memory expansion capabilities offer a 1 megabyte addressing range. The dynamic relocation scheme allows ease in segmentation of pure procedure and data for efficient memory utilization. Four segment registers (code, stack, data, extra) contain program loaded offset values which are used to map 16-bit addresses to 20-bit addresses. Each register maps 64K bytes at a time with activation of a specific register controlled explicity by program control and selected implicity by specific functions and instructions. All Intel languages support the extended memory capability, relieving the programmer of managing the megabyte memory space yet allowing explicit control when necessary.

Memory Configuration

The iSBC 86/05A microcomputer contains 8K bytes of high-speed 8K x 4 bit static RAM on-board. In addition, the above on-board RAM may be expanded to 16K bytes with the iSBC 302 MULTIMODULE RAM option which mounts on the iSBC 86/05A board. All on-board RAM is accessed by the 8086-2 CPU with no wait states, yielding a memory cycle time of 500 ns.

The iSBC 86/05A board also has four 28-pin, 8-bit wide (byte-wide) sockets, configured to accept JEDEC 24/28-pin standard memory devices. Up to 256K bytes of EPROM are supported in 64K byte increments with Intel 27512 EPROMs. The iSBC 86/05A board also supports 2K x 8, 4K x 8, 8K x 8, 16K x 8 and 32K x 8 EPROM memory devices. These sites also support 2K x 8 and 8K x 8 byte-wide static RAM (SRAM) devices and iRAM devices, yielding up to 32K bytes of SRAM in 8K byte increments on the baseboard.

When the addition of the iSBC 341 MULTIMODULE EPROM option, the on-board capacity for these devices is doubled, providing up to 512K bytes of EPROM and 64K bytes of byte-wide SRAM capacity on-board.

Parallel I/O Interface

The iSBC 86/05A Single Board Computer contains 24 programmable parallel I/O lines implemented using the Intel 8255A Programmable Peripheral Interface. The system software is used to configure the I/O lines in any combination of unidirectional input/output and bidirectional ports indicated in Table 1. In order to take advantage of the large number of possible I/O configurations, sockets are provided for interchangeable I/O line drivers and terminators, allowing the selection of the appropriate combination of optional line drivers and terminators with the required drive/termination characteristics. The 24 programmable I/O lines and signal ground lines are brought out to a 50-pin edge connector.

Serial I/O

A programmable communications interface using the Intel 8251A Universal Synchronous/Asynchronous Receiver/Transmitter (USART) is contained on the iSBC 86/05A board. A software selectable baud rate generator provides the USART with all common communication frequencies. The mode of operation (i.e., synchronous or asynchronous), data format, control character format, parity, and baud rate are all under program control. The 8251A provides full duplex, double buffered transmit and receive capability. Parity, overrun, and framing error detection are all

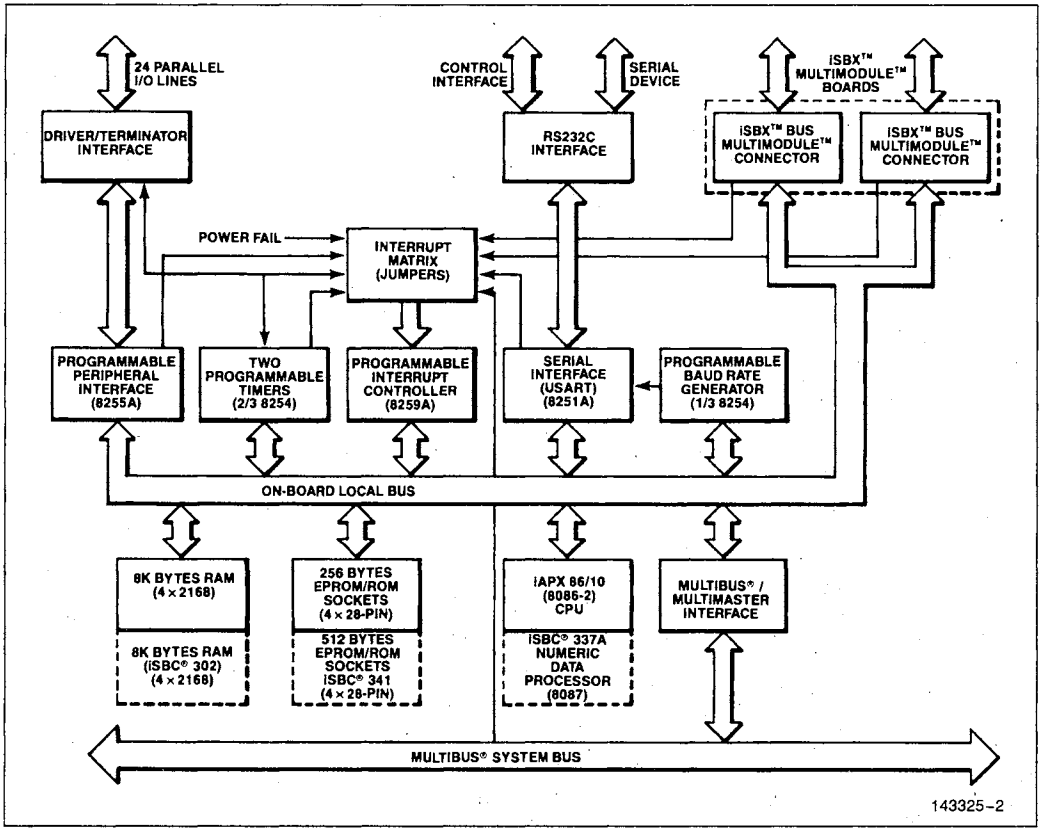


Figure 1. iSBC® 86/05A Block Diagram

incorporated in the USART. The RS232C compatible interface in conjunction with the USART, provides a direct interface to RS232C compatible terminals, cassettes, and asynchronous/synchronous modems. The RS232C command lines, serial data lines and signal ground line are brought out to a 26-pin edge connector.

Programmable Timers

The iSBC 86/05A board provides three independent, fully programmable 16-bit interval timers/event counters utilizing the Intel 8254 Programmable Interval Timer. Each counter is capable of operating in either BCD or binary modes. Two of these timers/counters are available to the systems designer to generate accurate time intervals under software control. Routing for the outputs and gate/trigger inputs of two of these counters is jumper selectable. The outputs may be independently routed to the 8259A Programmable Interrupt Controller and to the I/O terminators associated with the 8255A to allow external devices or an 8255A port to gate the timer or to count external events. The third interval timer in the 8254 provides the programmable baud rate generator for the iSBC 86/05A board RS232C USART serial port. The system software configures each timer independently to select the desired function. Seven functions are available as shown in Table 2. The contents of each counter may be read at any time during system operation.

iSBX™ MULTIMODULE™ On-Board Expansion

Two 8/16-bit iSBX MULTIMODULE connectors are provided on the iSBC 86/05A microcomputer. Through these connectors, additional on-board I/O and memory functions may be added. iSBX MULTIMODULE boards support functions such as additional parallel and serial I/O, analog I/O, mass storage device controllers (e.g., cassettes and floppy disks), BITBUS™ controllers, bubble memory, and other custom interfaces to meet specific needs. By mounting directly on the single board computer, less inter-

Table 1. Input/Output Port Modes of Operation

Port	Lines (qty)	Mode of Operation					Control
		Unidirectional				Bidirectional	
		Input		Output			
		Latched	Latched & Strobed	Latched	Latcched & Strobed		
1	8	X	X	X	X	X	
2	8	X	X	X	X		
3	4	X		X			X[1]
	4	X		X			X[1]

NOTE:
1. Part of port 3 must be used as a control port when either port 1 or port 2 are used as a latched and strobed input or a latched and strobed output port or port 1 is used as a bidirectional port.

Table 2. Programmable Timer Functions

Function	Operation
Interrupt on Terminal Count	When Terminal Count is Reached, an Interrupt Request is Generated. This Function is Extremely Useful for Generation of Real-Time Clocks.
Programmable One-Shot	Output Goes Low upon Receipt of an External Trigger Edge or Software Command and Returns High when Terminal Count is Reached. This Function is Retriggerable.
Rate Generator	Divide by N Counter. The Output will go Low for One Input Clock Cycle, and the Period from One Low Going Pulse to the Next is N Times the Input Clock Period.
Square-Wave Rate Generator	Output will Remain High Until One-Half the Count has been Completed, and go Low for the Other Half of the Count.
Software Triggered Strobe	Output Remains High Until Software Loads Count (N). N Counts After Count is Loaded, Output goes Low for One Input Clock Period.
Hardware Triggered Strobe	Output Goes Low for One Clock Period N Counts After Rising Edge Counter Trigger Input. The Counter is Retriggerable.
Event Counter	On a Jumper Selectable Basis, the Clock Input Becomes an Input from the External System. CPU may Read the Number of Events Occurring After the Counter "Window" has been Enabled or an Interrupt may be Generated After N Events Occur in the System.

face logic, less power, simpler packaging, higher performance, and lower cost result when compared to other alternatives such as MULTIBUS form factor compatible boards. The iSBX connectors on the iSBC 86/05A board provide all signals necessary to interface to the local on-board bus, including 16 data lines for maximum data transfer rates. iSBX MULTIMODULE boards designed with 8-bit data paths and using the 8-bit iSBX connector are also supported on the iSBC 86/05A microcomputer. A broad range of iSBX MULTIMODULE options are available in this family from Intel. Custom iSBX modules may also be designed for use on the iSBC 86/05A board. An iSBX bus interface specification is available from Intel.

MULTIBUS SYSTEM BUS AND MULTIMASTER CAPABILITIES

Overview

The MULTIBUS system bus (IEEE 796) is Intel's industry standard microcomputer bus structure. Both 8- and 16-bit single board computers are supported on the MULTIBUS structure with 24 address and 16 data lines. In its simplest application, the MULTIBUS system bus allows expansion of functions already contained on a single board computer (e.g., memory and digital I/O). However, the MULTIBUS structure also allows very powerful distributed processing configurations with multiple processors and intelligent slave I/O, and peripheral boards capable of solving the most demanding microcomputer applications. The MULTIBUS system bus is supported with a broad array of board level products, LSI interface components, detailed published specifications and application notes.

Expansion Capabilities

Memory and I/O capacity may be expanded and additional functions added using Intel MULTIBUS compatible expansion boards. Memory may be expanded by adding user specified combinations of RAM boards, EPROM boards, or combination boards. Input/output capacity may be added with digital I/O and analog I/O expansion boards. Mass storage capability may be achieved by adding single or double density diskette controllers, or hard disk controllers.

Multimaster Capabilities

For those applications requiring additional processing capacity and the benefits of multiprocessing (i.e., several CPUs and/or controllers logically sharing system tasks through communication of the system bus), the iSBC 86/05A board provides full MULTIBUS arbitration control logic. This control logic allows up to three iSBC 86/05A boards or other bus masters to share the system bus using a serial (daisy chain) priority scheme and allows up to 16 masters to share the MULTIBUS system bus with an external parallel priority decoder. In addition to the multiprocessing configurations made possible with multimaster capability, it also provides a very efficient mechanism for all forms of DMA (Direct Memory Access) transfers.

Interrupt Capability

The iSBC 86/05A board provides 9 vectored interrupt levels. The highest level is the NMI (Non-Maskable Interrupt) line which is directly tied to the 8086 CPU. This interrupt is typically used for signaling catastrophic events (e.g., power failure). The Intel 8259A Programmable Interrupt Controller (PIC) provides control and vectoring for the next eight interrupt levels. As shown in Table 3, a selection of four priority processing modes is available for use in designing request processing configurations to match system requirements for efficient interrupt servicing with minimal latencies. Operating mode and priority assignments may be reconfigured dynamically via software at any time during system operation. The PIC accepts interrupt requests from all on-board I/O resources and from the MULTIBUS system bus. The PIC then resolves requests according to the selected mode and, if appropriate, issues an interrupt to the CPU. Any combination of interrupt levels may be masked via software, by storing a single byte in the interrupt mask register of the PIC. In systems requiring additional interrupt levels, slave 8259A PICs may be interfaced via the MULTIBUS system bus, to generate additional vector addresses, yielding a total of 65 unique interrupt levels.

Interrupt Request Generation

Interrupt requests to be serviced by the iSBC 86/05A board may originate from 24 sources. Table 4 includes a list of devices and functions supported by interrupts. All interrupt signals are brought to the interrupt jumper matrix where any combination of interrupt sources may be strapped to the desired interrupt request level on the 8259A PIC or the NMI input to the CPU directly.

Power-Fail Control and Auxiliary Power

Control logic is also included, to accept a power-fail interrupt in conjunction with a power-supply having AC-low signal generation capabilities, to initiate an orderly shut down of the system in the event of a power failure. Additionally, an active-low TTL compatible memory protect signal is brought out on the auxiliary connector which, when asserted, disables read/write access to RAM for systems requiring battery backup of read/write memory. Selection of this auxiliary RAM power bus is made via jumpers on the board.

Table 3. Programmable Interrupt Modes

Mode	Operation
Fully Nested	Interrupt Request Line Priorities Fixed at 0 as Highest, 7 as Lowest.
Auto-Rotating	Equal Priority. Each Level, After Receiving Service, Becomes the Lowest Priority Level until next Interrupt Occurs.
Specific Priority	System Software Assigns Lowest Priority Level. Priority of all Other Levels Based in Sequence Numerically on this Assignment.
Polled	System Software Examines Priority-Encoded System Interrupt Status via Interrupt Status Register.

Table 4. Interrupt Request Sources

Device	Function	Number of Interrupts
MULTIBUS Bus Interface	Requests from MULTIBUS Resident Peripherals or Other CPU Boards	8; may be Expanded to 64 with Slave 8259A PICs on MULTIBUS Boards
8255A Programmable Peripheral Interface	Signals Input Buffer Full or Output Buffer Empty; also BUS INTR OUT General Purpose Interrupt from Driver/Terminator Sockets	3
8251A USART	Transmit Buffer Empty and Receive Buffer Full	2
8254 Timers	Timer 0, 1 Outputs; Function Determined by Timer Mode	2
iSBX Connectors	Function Determined by iSBX MULTIMODULE Board	4 (2 per iSBX Connector)
Bus Fail Safe Timer	Indicates Addressed MULTIBUS Resident Device has not Responded to Command within 6–10 ms	1
Power Fail Interrupt	Indicates AC Power is not within Tolerance	1
Power Line Clock	Source of 120 Hz Signal from Power Supply	1
External Interrupt	General Purpose Interrupt from Auxiliary (P2) Connector on Backplane	1
iSBC 337A MULTIMODULE Numeric Data Processor	Indicates Error or Exception Condition	1

System Development Environment

Development support for the iSBC 86/05A Board is offered on the System 310 and Series IV Microcomputer Development System from Intel as well as the IBM Personal Computer.

In the Series IV, System 310 and IBM PC development environments, languages offered are Assembler, PLM-86, C, Fortran and Pascal. A powerful software debugger, PSCOPE, is also offered on all development systems. PSCOPE provides Software Trace Execution, defineable breakpoints and user defined/executable debugging procedures.

In-Circuit Emulator

The I²ICE™ In-Circuit Emulator provides the necessary link between the software development environment and the "target" iSBC 86/05A board, the I²ICE In-Circuit Emulator provides a sophisticated command set to assist in debugging software and final integration of the user hardware and software.

iSDM™ System Debug Monitor

The Intel iSDM System Debug Monitor package contains the necessary hardware, software, cables, EPROMs and documentation required to interface, through a serial or parallel connection, an iSBC 86/05A target system to System 310 or Series IV Intellec® Microcomputer Development System for execution and interactive debugging of applications software on the target system. The Monitor can: load programs into the target system; execute the programs instruction by instruction or at full speed; set breakpoints; and examine/modify CPU registers, memory content, and other crucial environmental details. Additional custom commands can be built using the Command Extension Interface (CEI).

Software Support

The iRMX 86 operating system is offered for development with a System 310 and provides users with a powerful set of system building blocks for developing many different real-time applications. Key iRMX 86 operating system features include multitasking, multiprogramming, interrupt management, device independence, file protection and control, interactive debugging, plus interfaces to many Intel and non-Intel developed hardware and software products.

The iRMX 86 operating system is highly modular and configurable, and includes a sophisticated file management, I/O system, and powerful human interface. The iRMX 86 operating system is also easily customized and extended by the user to match unique requirements.

SPECIFICATIONS

Word Size

Instruction: 8, 16, 24, or 32 bits
Data: 8, 16 bits

System Clock

5.00 MHz or 8.00 MHz ± 0.1% (jumper selectable)

Basic Instruction Cycle

At 8 MHz: 750 ns
250 ns (assumes instruction in the queue)
At 5 MHz: 1.2 sec.
400 ns (assumes instruction in the queue)

NOTE:
Basic instruction cycle is defined as the fastest instruction time (i.e., two clock cycles).

Memory Cycle Time

500 ns cycle time (no wait states requires a memory component access time of 250 ns or less)
RAM: 500 ns
EPROM: Jumper selectable from 500 ns to 875 ns

Memory Capacity/Addressing

JEDEC 24/28 Pin Sites		
Device	**Total Capacity**	**Address Range**
2K × 8	8K bytes	FE000-FFFFF$_H$
4K × 8	16K bytes	FC000-FFFFF$_H$
8K × 8	32K bytes	F8000-FFFFF$_H$
16K × 8	64K bytes	F0000-FFFFF$_H$
32K × 8	128K bytes	E0000-FFFFF$_H$
64K × 8	256K bytes	C0000-FFFFF$_H$
With iSBC® 341 MULTIMODULE™ EPROM/SRAM		
Device	**Total Capacity**	**Address Range**
2K × 8	16K bytes	FC000-FFFFF$_H$
4K × 8	32K bytes	F8000-FFFFF$_H$
8K × 8	64K bytes	F0000-FFFFF$_H$
16K × 8	128K bytes	E0000-FFFFF$_H$
32K × 8	256K bytes	C0000-FFFFF$_H$
64K × 8	512K bytes	80000-FFFFF$_H$

NOTE:
iSBC 86/05A EPROM sockets support JEDEC 24/28-pin standard EPROMs and RAMS.

ON-BOARD STATIC RAM

8K bytes — 0-1FFF$_H$

16K bytes— 0-3FFF$_H$ (with iSBC 302 MULTIMODULE Board)

I/O CAPACITY

PARALLEL — 24 programmable lines using one 8255A.

SERIAL — 1 programmable line using one 8251A.

iSBX MULTIMODULE— 2 iSBX single wide MULTIMODULE board or 1 iSBX double-width MULTIMODULE board.

SERIAL COMMUNICATIONS CHARACTERISTICS

SYNCHRONOUS — 5-8 bit characters; internal or external character synchronization; automatic sync insertion.

ASYNCHRONOUS— 5-8 bit characters; break character generation; 1, 1½, or 2 stop bits; false start bit direction.

Baud Rates

Frequency (KHz) (Software Selectable)	Baud Rate (Hz)		
	Synchronous	Asynchronous	
		÷16	÷64
153.6	—	9600	2400
76.8	—	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
2.4	2400	150	—
1.76	1760	110	—

NOTE:
1. Frequency selected by I/O write of appropriate 16-bit frequency factor to baud rate register (8254 Timer 2).

TIMERS

Input Frequencies

Reference: 2.46 MHz ±0.1% (0.041 sec. period, nominal); or 153.60 KHz ±0.1% (6.51 sec. period, nominal)

NOTE:
Above frequencies are user selectable

Event Rate: 2.46 MHz max

Output Frequencies/Timing Intervals

Function	Single Timer/Counter		Dual Timer/Counter (Two Timers Cascaded)	
	Min	Max	Min	Max
Real-Time Interrupt	1.63 µs	427.1 ms	3.26s	466.50 min
Programmable One-Shot	1.63 µs	427.1 ms	3.26s	466.50 min
Rate Generator	2.342 Hz	613.5 kHz	0.000036 Hz	306.8 kHz
Square-Wave Rate Generator	2.342 Hz	613.5 kHz	0.000036 Hz	306.8 kHz
Software Triggered Strobe	1.63 µs	427.1 ms	3.26s	466.50 min
Hardware Triggered Strobe	1.63 µs	427.1 ms	3.26s	466.50 min
Event Counter	—	2.46 MHz	—	—

INTERFACES

MULTIBUS Bus:	All signals TTL compatible
iSBX BUS Bus:	All signals TTL compatible
PARALLEL I/O:	All signals TTL compatible
SERIAL I/O:	RS232C compatible, configurable as a data set or data terminal
TIMER:	All signals TTL compatible
INTERRUPT REQUESTS:	All TTL compatible

Connectors

Interface	Double-Sided Pins (qty)	Centers (in.)	Mating Connectors
MULTIBUS System	86	0.156	Viking Wire Wrap
iSBX Bus			
8-Bit Data	36	0.1	iSBX 960-5
16-Bit Data	44	0.1	iSBX 961-5
Parallel I/O (2)	50	0.1	3M Flat or T1 PINS
Serial I/O	26	0.1	3M Flat or AMP Flat

LINE DRIVERS AND TERMINATORS

I/O Drivers

The following line drivers are all compatible with the I/O driver sockets on the iSBC 86/05A board.

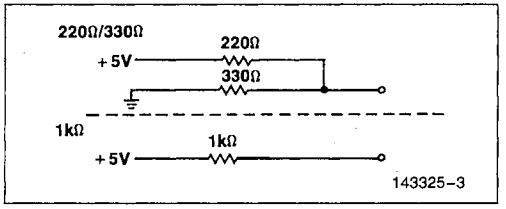
Driver	Characteristic	Sink Current (mA)
7438	I,OC	48
7437	I	48
7432	NI	16
7426	I,OC	16
7409	NI,OC	16
7408	NI	16
7403	I,OC	16
7400	I	16

NOTES:
I = inverting; NI = non-inverting; OC = open collector.

Port 1 of the 8255A has 20 mA totem-pole bidirectional drivers and 1K terminators

I/O Terminators

220/330 divider or 1K pullup



MULTIBUS® DRIVERS

Function	Characteristic	Sink Current (mA)
Data	Tri-State	50
Address	Tri-State	50
Commands	Tri-State	32
Bus Control	Open Collector	20

Physical Characteristics

Width: 12.00 in. (30.48 cm)
Height: 6.75 in. (17.15 cm)
Depth: 0.70 in. (1.78 cm)
Weight: 14 oz (388 gm)

ELECTRICAL CHARACTERISTICS

DC Power Requirements

Configuration	Current Requirements (All Voltages ±5%)		
	+5V	+12V	−12V
Without EPROM[1] RAM only[2]	4.7A 120 mA	25 mA	23 mA
With 8K EPROM[3] (using 2716)	5.0A	25 mA	23 mA
With 16K EPROM[3] (using 2732)	4.9A	25 mA	23 mA
With 32K EPROM[3] (using 2764)	4.9A	25 mA	23 mA

NOTES:
1. Does not include power for optional ROM/EPROM, I/O drivers, and I/O terminators.
2. RAM chips powered via auxiliary power bus in power-down mode.
3. Includes power required for 4 ROM/EPROM chips, and I/O terminators installed for 16 I/O lines; all terminator inputs low.

ENVIRONMENTAL CHARACTERISTICS

Operating Temperature: 0°C to 55°C

Relative Humidity: to 90% (without condensation)

REFERENCE MANUAL

Order no. 147162-002—*iSBC 86/05A Hardware Reference Manual* (NOT SUPPLIED)

Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDER INFORMATION

Part Number	Description
SBC 86/05A	16-bit Single Board Computer with 8K bytes RAM