iSBC™ 550 ETHERNET COMMUNICATIONS CONTROLLER HARDWARE REFERENCE MANUAL

Order Number: 121746-001

Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051

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PREFACE

This manual, which is intended for the design engineer, programmer, or technician who will install and maintain the iSBC 550 Ethernet Communications Controller, is divided into the following six chapters:

- Chapter 1, *General Description*, includes a brief description of the controller boards and the Ethernet architecture. Included are salient specifications for the controller.
- Chapter 2, *Preparation for Use*, provides information on unpacking, installing, and testing the controller.
- Chapter 3, *Functional Overview*, describes the architecture of the controller and the hardware implementation of the various operating sequences.
- Chapter 4, *Processor Board Theory of Operation*, describes the logic and timing involved in executing the overall functions of the processor board.
- Chapter 5, *SerDes Board Theory of Operation*, describes the logic and timing involved in transmitting and receiving data packets and verifying the SerDes board and transceiver.
- Chapter 6, *Service Information*, provides the controller service diagrams, lists its replaceable parts, and describes how to obtain service and repair assistance. Also included is a brief description of the firmware-based confidence test.

Supporting documentation on the Ethernet is available in the following documents:

- *Ethernet Communications Controller Programmer's Reference Manual*, Order No. 121769
- *The Ethernet Data Link Layer and Physical Layer Specifications*, Order No. 121794.

CONTENTS

CONTENTS (Cont'd.)

TABLES

ILLUSTRATIONS

CHAPTER 1
GENERAL INFORMATION

1-1. INTRODUCTION

The iSBC 550 Ethernet Communications Controller provides a high-speed local area network interface for any Intel MCS-85, iAPX 86, or iAPX 88 based microcomputer application. This Multibus interface compatible controller provides support for the Ethernet Data Link and Physical Link Control to comply with the Ethernet specification of a 10-megabit per second transmission rate over coaxial cable.

1-2. DESCRIPTION

The iSBC 550 Ethernet Communications Controller (figure 1-1) consists of a processor board and a serialization/deserialization (SerDes) board. The processor board includes firmware to manage packet encapsulation, buffering, processing, and transferring processed packets to system memory. The SerDes board performs the serialization/deserialization, framing, CRC generation and checking, Manchester encoding and decoding, destination address recognization, and the functions required to implement the carrier-sense multiple-access with collision-detection (CSMA/CD) link access protocol associated with *The Ethernet Data Link Layer and Physical Link Layer Specifications*, developed jointly by the Intel, Xerox, and Digital Equipment Corporations.

1-3. PROCESSOR BOARD

The Intel 5-MHz 8088-based processor board, which provides the interface to the Multibus (system bus), contains 8k bytes of firmware preprogrammed for the Data Link Layer (DLL) and Multibus Interprocessor Protocol (MIP) interface. The MIP interface is also implemented by the iMMX Multibus Message Exchange software package for the ISIS-II Operating System and iRMX Real-Time Executives.

Ethernet commands and messages are sent by the host system CPU to the processor board via the system bus. The controller board analyzes and executes these commands under firmware control of

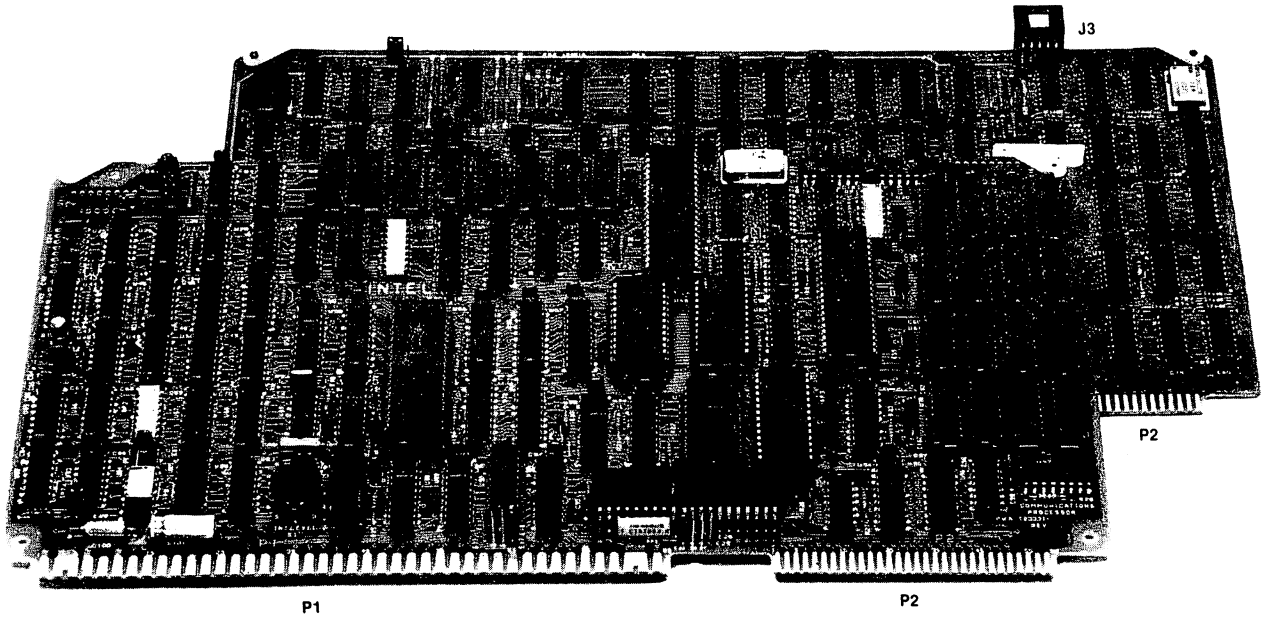


Figure 1-1. iSBC 550 Ethernet Communications Controller 121746-1

the onboard 8088 CPU. In addition, the firmware monitors the status of the SerDes board and controls the reception and transmission of data packets into and out of buffer memory. All data transfers from the SerDes board are DMA buffered through the 8k bytes of static RAM on the processor board. The DMA capability minimizes the amount of system bus time used by the iSBC 550 controller and eliminates the possibility of data overruns and subsequent repeated I/O operations. The buffer also allows the iSBC 550 controller to have bus priority below that of other higher-priority, time-critical controllers in the system.

A firmware-resident confidence test, which provides a fundamental level of controller integrity, is invoked automatically on power-up or system reset. The test functions include (1) testing the processor onboard memory and LSI chips, (2) sending packets with bad and good CRC, (3) receiving all packets regardless of address, (4) reading data received in error, and (5) SerDes loop- back. The SerDes loop-back function allows data from static RAM to be transmitted and received at the same time; although the received data is not written to the static RAM memory, the CRC checking verifies the formatting, transmission and reception of data.

1-4. SERDES BOARD

The SerDes board provides the required electrical characteristics of the Physical Link Layer of the Ethernet architecture for a transceiver interface. The major functions of the SerDes board include serialization/deserialization, packet framing, Manchester encoding/decoding, transmit data flow control, receive data flow control, destination address decoding for received message, CRC generation and checking, and diagnostics for CRC error, loopback, transmit timeout, and link access control using the CSMA/CD (carrier-sense multiple-access with collision detection) protocol.

1-5. ETHERNET ARCHITECTURE

The Ethernet architecture defines the system as a series of independent layers, the lowest of which is the Physical Link Layer concerned with coaxial cable interface. The Data Link Layer supports the peer protocol statistical contention resolution (CSMA/CD), variable size frames, and link management functions. The precise definition for these two layers can be found in *The Ethernet Data Link Layer and Physical Link Layer Specifications*, developed jointly by Intel, Xerox, and Digital Equipment Corporation.

The higher levels of the overall architecture that use the Data Link Layer are outside the standard definition. Typically, the user supplies the Transport Control Layer, Session Control Layer, and the Presentation and Application Layers, commonly referred to as the Client Layer. The Transport Control Layer is concerned with the end-to-end communications and the virtual channel connection via a port-to-port address. The Session Control Layer provides the process-to-process control function which includes the symbolic name binding and the establishment of the virtual connection via the Transport Control Layer. The exact error and recovery control are application specific.

1-6. CONTROLLER SPECIFICATIONS

Specifications of the iSBC 550 Ethernet Communications Controller are listed in table 1-1.

1-7. KIT CONTENTS

The following items are supplied with the iSBC 550 Ethernet Communications Controller:

Item 1. iSBC 550 Communications Processor Board, Part No. 123331

Item 2. iSBC 550 Communications SerDes Board, Part No. 124016

Item 3. Internal Transceiver Cable, Part No. 123591

Item 4. Dual Auxiliary Connector, Part No. 1000751

Item 5. Dual Auxiliary Connector, Part No. 1000515

Item 6. Communications Processor Board Schematic Diagram

Item 7. Communications SerDes Board Schematic Diagram

Item 8. Accessory Kit Assembly, Part No. 124351

The accessory kit assembly consists of an internal transceive cable and assorted hardware. The hardware is to be used to attach the internal transceiver cable connector to the rear panel of an Intellec Microcomputer Development System.

Table 1-1. Controller Specifications

ONBOARD MEMORY

Dynamic RAM:	16k bytes used primarily for storage of code downloaded from system memory.
Static RAM:	8k bytes used as buffer for packet transmission and reception.
EPROM:	8k bytes of firmware for External Data Link (EDL), Data Link Layer (DLL), Multibus Interprocessor Protocol (MIP), bootstrap, and confidence test.

MEMORY ADDRESSING

Dynamic RAM:	F0000-F3FFFH.
Static RAM:	F8000-F9FFFH.
EPROM:	FE000-FFFFFH.
System:	00000-EFFFFH.

SYSTEM CLOCK: 5 MHz ±0.1%.

I/O CHANNEL CAPACITY: One Ethernet compatible serial channel to user-supplied transceiver.

FRAME SIZE: 64-bit *preamble*, 48-bit *destination address*, 48-bit *source address*, 16-bit *type*, 46-1500 bytes for *data*, and 32-bit *frame check sequence*.

INTERFACES

System Bus:	Multibus compatible; TTL level.
Transceiver:	Ethernet transceiver compatible; series 10,000 ECL level.

ENVIRONMENTAL REQUIREMENTS

Operating Temperature:	0° to 55°C (32° to 131°F).
Relative Humidity:	To 90% without condensation.

PHYSICAL CHARACTERISTICS

Width (each board):	30.48 cm (12.00 inches).
Height (each board):	17.15 cm (6.75 inches).
Thickness (each board):	1.78 cm (0.7 inch).
Weight (both boards):	1.6 kg (3.5 pounds).

POWER REQUIREMENTS: +5V dc at 9.0A maximum
+12V dc at 0.5A maximum.

BASIC NETWORK REQUIREMENTS

Coaxial Cable Length:	500 meters (1640.42 feet) maximum.
Transceiver Cable Length:	50 meters (164 feet) maximum.
Number of Stations:	100 maximum.
Baud Rate:	10 megabits/second.

MATING CONNECTOR REQUIREMENTS:

Function	No. of Pairs/Pins	Centers (Inches)	Vendor	Vendor Part No.
Multibus Interface (P1)	43/86	0.156	Viking ELFAB	2KH43/9AMK12 (solder type) BW1562A43PBB (wirewrap type)
Auxiliary (P2)	Connector	P2-P2 connector is supplied.		
Transceiver Interface (P3)	A 0.55-meter (22-inch) internal transceiver cable is supplied. Transceiver end of cable requires 15-pin male mating delta connector: Shell: AMP 205206-1 Crimp Contact: AMP 66506-4			

CHAPTER 2
PREPARATION FOR USE

2-1. INTRODUCTION

This chapter provides instructions for preparing the iSBC 550 Ethernet Communications Controller for use in the user-defined environment.

2-2. UNPACKING AND INSPECTION

Inspect the shipping carton immediately upon receipt for evidence of mishandling during transit. If the shipping carton is severely damaged or waterstained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is not present when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, contact the Intel Technical Support Center (see paragraph 6-3) to obtain a Return Authorization Number and further instructions. A purchase order will be required to complete the repair. A copy of the purchase order should be submitted to the carrier with your claim.

It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be reshipped.

Carefully unpack the shipping carton and verify that the items listed below are included. Compare the packing slip with your purchase order to verify that the order is complete. The carton and packing materials should be saved in case it becomes necessary to reship the controller at a later date.

2-3. INSTALLATION CONSIDERATIONS

The controller is designed for installation into the Intel iSBC 604/614 Modular Backplane and Cardcage as found in the Series 80 single board computer mainframes. The controller can also be installed in an Intellec Model 800 or any of the Intellec series of Microcomputer Development Systems. The controller additionally can be installed into a user's Multibus-compatible backplane assembly that meets the dimensional requirements of the controller's mating connectors.

2-4. POWER REQUIREMENTS

The controller requires power supplies of +5V (±0.25V) at 9.0A maximum and ±12V (±0.6V) at 0.5A maximum. Before installing the controller, ensure that the system power supply can safely meet this additional current demand. The power supply capacities of the Intellec Model 800 and Intellec Series II/III Microcomputer Development Systems are given in the following documents:

a. *Intellec Model 800 Hardware Reference Manual*, Order No. 9800132

b. *Intellec Series II Model 22X/23X Installation Manual*, Order No. 9800559

c. *Intellec Series III Microcomputer Development Installation and Checkout Manual*, Order No. 121612

2-5. COOLING REQUIREMENTS

The controller dissipates 710 gram-calories per minute (2.87 Btu/minute). The iSBC 80 Series mainframes, Intellec 800, and the Intellec Microcomputer Development Systems provide forced-air cooling that is generally adequate to maintain an internal operating temperature below 131°F (55°C). When installing the controller in a high-temperature environment or in any other system enclosure, ensure that the internal operating temperature is not permitted to exceed the 131°F (55°C) maximum.

2-6. PHYSICAL DIMENSIONS

The processor board and SerDes board have the same physical dimensions as follows:

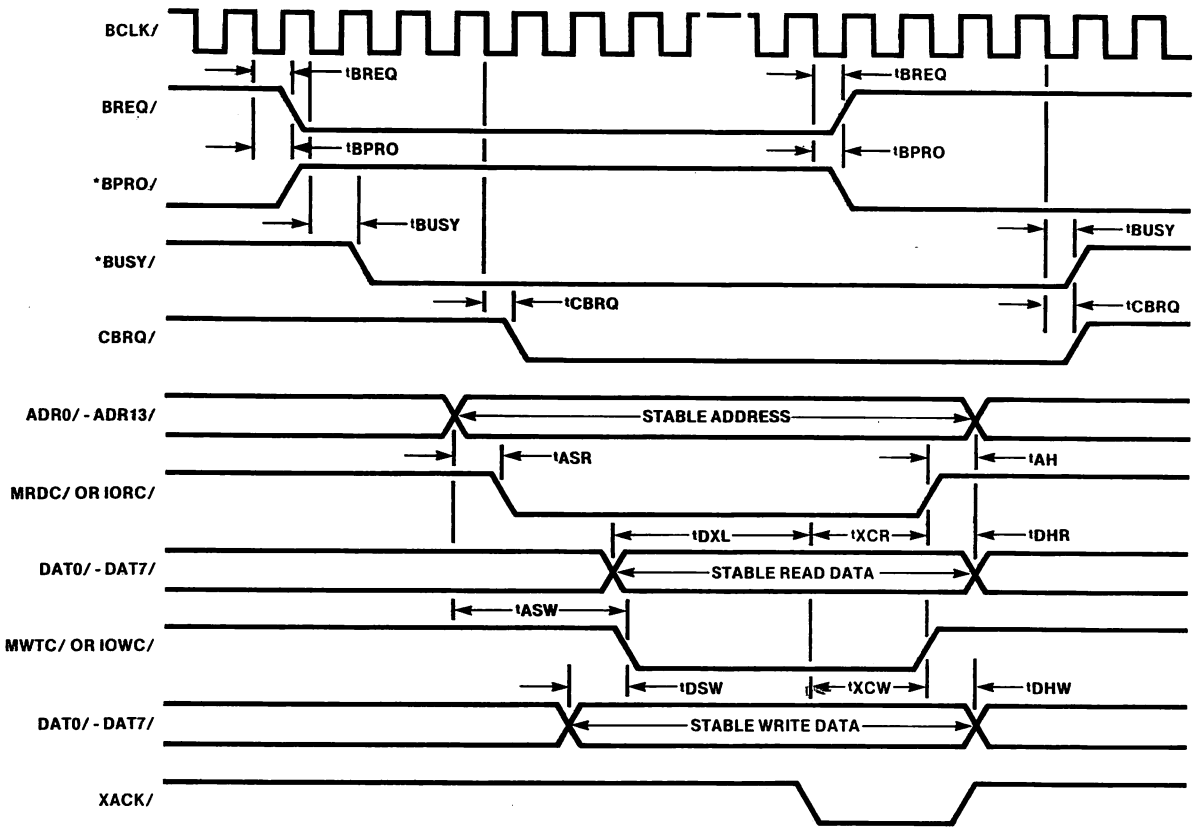
a. Width: 12.00 inches (30.48 cm)

b. Height: 6.75 inches (17.15 cm)

c. Thickness: 0.70 inch (1.78 cm)

2-7. MULTIBUS INTERFACE

The controller communicates with the host system processor, system I/O, and system memory via the Multibus interface. Tables 2-1, 2-2 and 2-3 define the Multibus interface pin assignments, signal functions, and dc characteristics, respectively. The controller connects to the Multibus interface through connector P1, which is an 86-pin, double-sided, printed-circuit edge connector with 0.156-inch (3.96-millimeter) contact centers. The bus acquisition and data transfer timing is illustrated in figure 2-1.



*ASSUMES BPRN/ ACTIVE

Parameter	Minimum	Maximum	Description
tCBRQ	67 ns		BCLK/ to CBRQ/ Delay
tBCY	100 ns		Bus Clock Period
tBW	35 ns		Bus Clock Pulse Width
tBREQ		35 ns	BCLK/ to BREQ/ Delay
tBPRNS	22 ns		BPRN/ to BCLK/ Setup Time
tBPRO		40 ns	BCLK/ to BPRO/ Delay
tBPRN		30 ns	BPRN/ to BPRO/ Delay
tBUSY		55 ns	BCLK/ to BUSY/ Low Delay
tASR	286 ns		Address Setup Time (Read)
tAH	147 ns		Address Hold Time
tDXL	−250 ns		Data Setup to Acknowledge Time (Read)
tXCR	567 ns	1327 ns	Acknowledge to Command High (Read)
tDHR	−80 ns		Data Hold Time (Read)
tASW	786 ns		Address Setup Time (Write)
tDSW	80 ns		Data Setup to Command Time (Write)
tXCW	567 ns	1257 ns	Acknowledge to Command High (Write)
tDHW	65 ns		Data Hold Time (Write)
tINIT	4 ns		Reset pulse Width

Figure 2-1. Bus Acquisition and Data Transfer Timing

121746-2

Table 2-1. Connector P1 Pin Assignments

	Pin	(Component Side)		Pin	(Circuit Side)	
		Mnemonic	Description		Mnemonic	Description
POWER SUPPLIES	1	GND	Signal GND	2	GND	Signal GND
	3	+5V	+5Vdc	4	+5V	+5Vdc
	5	+5V	+5Vdc	6	+5V	+5Vdc
	7	+12V	+12Vdc	8	+12V	+12Vdc
	9		Reserved	10		Reserved
	11	GND	Signal GND	12	GND	Signal GND
BUS CONTROLS	13	BCLK/	Bus Clock	14	INIT/	Initialize
	15	BPRN/	Bus Priority In	16	BPRO/	Bus Priority Out
	17	BUSY/	Bus Busy -	18	BREQ/	Bus Request
	19	MRDC/	Mem Read Cmd	20	MWTC/	Mem Write Cmd
	21	IORC/	I/O Read Cmd	22	IOWC/	I/O Write Cmd
	23	XACK/	XFER Acknowledge	24		Reserved
BUS CONTROLS AND ADDRESS	25		Reserved	26		Reserved
	27		Reserved	28	ADR10/	
	29	CBRQ/	Common Bus Request	30	ADR11/	Address
	31	CCLK/	Constant Clock	32	ADR12/	Bus
	33		Reserved	34	ADR13/	
INTERRUPTS	35	INT6/		36	INT7/	
	37	INT4/	Interrupt	38	INT5/	Interrupt
	39	INT2/	Requests	40	INT3/	Requests
	41	INT0/		42	INT1/	
ADDRESS	43	ADRE/		44	ADRF/	
	45	ADRC/		46	ADRD/	
	47	ADRA/	Address	48	ADRB/	Address
	49	ADR8/	Bus	50	ADR9/	Bus
	51	ADR6/		52	ADR7/	
	53	ADR4/		54	ADR5/	
	55	ADR2/		56	ADR3/	
	57	ADR0/		58	ADR1/	
DATA	59		Reserved	60		Reserved
	61		Reserved	62		Reserved
	63		Reserved	64		Reserved
	65		Reserved	66		Reserved
	67	DAT6/	Data Bus	68	DAT7/	Data Bus
	69	DAT4/	Data Bus	70	DAT5/	Data Bus
	71	DAT2/	Data Bus	72	DAT3/	Data Bus
	73	DAT0/	Data Bus	74	DAT1/	Data Bus
POWER SUPPLIES	75	GND	Signal GND	76	GND	Signal GND
	77		Reserved	78		Reserved
	79		Reserved	80		Reserved
	81	+5V	+5Vdc	82	+5V	+5Vdc
	83	+5V	+5Vdc	84	+5V	+5Vdc
	85	GND	Signal GND	86	GND	Signal GND

NOTE: All odd-numbered pins (1, 3, 5...85) are on component side of the board. Pin 1 is the left-most pin when viewed from the component side of the board with the extractors at the top. All unassigned pins are reserved.

Table 2-2. Multibus Interface Signal Functions

Signal	Functional Description
ADR0/ADRF/ ADR10/-ADR13/	*Address.* These 20 lines transmit the address of the memory location or I/O port to be accessed. ADR13/ is the most-significant bit.
BCLK/	*Bus Clock.* Used to synchronize the bus contention logic on all bus masters.
BPRN/	*Bus Priority In.* Indicates to a particular bus master that no higher priority bus master is requesting use of the bus. BPRN/ is synchronized with BCLK/.
BPRO/	*Bus Priority Out.* In serial (daisy chain) priority resolution schemes, BPRO/ must be connected to the BPRN/ input of the bus master with the next lower bus priority.
BREQ/	*Bus Request.* In parallel priority resolution schemes, BREQ/ indicates that a particular bus master requires control of the bus for one or more data transfers. BREQ/ is synchronized with BCLK/.
BUSY/	*Bus Busy.* Indicates that the bus is in use and prevents all other bus masters from gaining control of the bus. BUSY/ is synchronized with BCLK/.
CBRQ/	*Common Bus Request.* Indicates that a bus master wishes control of the bus but does not presently have control. As soon as control of the bus is obtained, the requesting bus controller raises the CBRQ/ signal.
CCLK/	*Constant Clock.* Provides a clock signal of constant frequency for use as a master clock by other system modules.
DAT0/-DAT7/	*Data.* These 8 bidirectional data lines transmit and receive data to and from the addressed memory location or I/O port. DAT7/ is the most-significant bit.
INIT/	*Initialize.* Resets the entire system to a known internal state.
INT0/-INT7/	*Interrupt Request.* These eight lines transmit Interrupt Requests to the appropriate interrupt handler. INT0 has the highest priority.
IORC/	*I/O Read Command.* Indicates that the address of an I/O port is on the address lines and that the output of that port is to be read (placed) onto the data lines.
IOWC/	*I/O Write Command.* Indicates that the address of an I/O port is on the address lines and that the contents on the data lines are to be accepted by the addressed port.
MRDC/	*Memory Read Command.* Indicates that the address of a memory location is on the address lines and that the contents of that location are to be read (placed) on the data lines.
MWTC/	*Memory Write Command.* Indicates that the address of a memory location is on the address lines and that the contents on the data lines are to be written into that location.
XACK/	*Transfer Acknowledge.* Indicates that the addressed memory location or I/O port has completed the specified read or write operation. That is, data has been placed onto or accepted from the data lines.

Table 2-3. Processor Board DC Characteristics

Signals	Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
XACK/	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.4V		−1.6	mA
	I_{IH}	Input Current at High V	V_{IN} = 2.4V		40	μA
	*C_L	Capacitive Load			15	pF
ADR0/-ADRF/ ADR10/-ADR13/	V_{OL}	Output Low Voltage	I_{OL} = 32 mA		0.45	V
	V_{OH}	Output High Voltage	I_{OH} = −5 mA	2.4		V
	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	*C_L	Capacitive Load			18	pF
BCLK/	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	*C_L	Capacitive Load			12	pF
BPRN/	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IH}	Input Current at High V	V_{IN} = 5.25V		60	μA
	*C_L	Capacitive Load			18	pF
BPRO/, BREQ/	V_{OL}	Output Low Voltage	I_{OL} = 20 mA		0.45	V
	V_{OH}	Output High Voltage	I_{OH} = −0.4 mA	2.4		V
	*C_L	Capacitive Load			12	pF
BUSY/, CBRQ/	V_{OL}	Output Low Voltage	I_{OL} = 20 mA		0.45	V
	I_{OL}	Input Current at High V	V_{IN} = 5.25V		60	μA
	V_{OH}	Output High Voltage	Open Collector			
	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	*C_L	Capacitive Load			12	pF
CCLK/	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	*C_L	Capacitive Load			15	pF
DAT0/-DAT7/	V_{OL}	Output Low Voltage	I_{OL} = 32 mA		0.45	V
	V_{OH}	Output High Voltage	I_{OH} = − mA	2.4		V
	V_{IL}	Input Low Voltage			0.80	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.45V		−0.20	mA
	I_{LH}	Output Leakage High	V_O = 5.25V		100	μA
	*C_L	Capacitive Load			18	pF
INIT/	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.4V		−4.2	mA
	I_{IH}	Input Current at High V	V_{IN} = 2.4V		−1.4	mA
	*C_L	Capacitive Load			15	pF
INT0/-INT7/	V_{IL}	Output Low Voltage			0.4	V
	V_{IH}	Output High Voltage		2.4		V

Table 2-3. Processor Board DC Characteristics (Cont'd.)

Signals	Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
IORC/, IOWC/	V_{OL}	Output Low Voltage	I_{OL} = 30 mA		0.45	V
	V_{OH}	Output High Voltage	I_{OH} = −5 mA	2.4		V
	V_{IL}	Input Low Voltage			0.95	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V			−2.0	mA
	I_{IH}	Input Current at High V	V_{In} = 5.25		1000	μA
	*C_L	Capacitive Load			25	pF
MRDC/, MWTC/	V_{OL}	Output Low Voltage	I_{OL} = 30 mA		0.45	V
	V_{OH}	Output High Voltage	I_{OH} = −5 mA	2.4		V
	*C_L	Capacitive Load			25	pF

*Capacitive load values are approximations.

2-8. BUS PRIORITY RESOLUTION

In a user-designed system, bus contention between two or more bus masters (e.g., the host system processor, communications processor board, disk/diskette controller, etc.) is implemented using a serial priority scheme.

The serial priority scheme employed in an iSBC 604 Cardcage is shown in figure 2-2. Due to the propagation delay of the BPRO/ signal path, this scheme is limited to a maximum of three bus masters capable of acquiring and controlling the bus. The bus master installed in slot J2 has the highest priority and is able to acquire control of the bus at any time because its BPRN/ input is always enabled (tied to ground) through jumpers B and N on the backplane.

If the bus master in slot J2 desires control of the bus, it drives its BPRO/ output high and inhibits the BPRN/ input to all lower-priority bus masters. When finished using the bus, the J2 bus master pulls its BPRO/ output low and gives the J3 bus master the opportunity to take control of the bus. If the J3 bus master does not desire to control the bus at this time, it pulls its BPRO/ output low and gives the lowest priority bus master in slot J5 the opportunity to assume control of the bus. Note in figure 2-2 that the SerDes board connects pin 15 to pin 16 to maintain the serial chain. Note also that a 1-kilohm pull-up resistor must be installed if the CBRQ/ line is used.

2-9. JUMPER/SWITCH CONFIGURATION

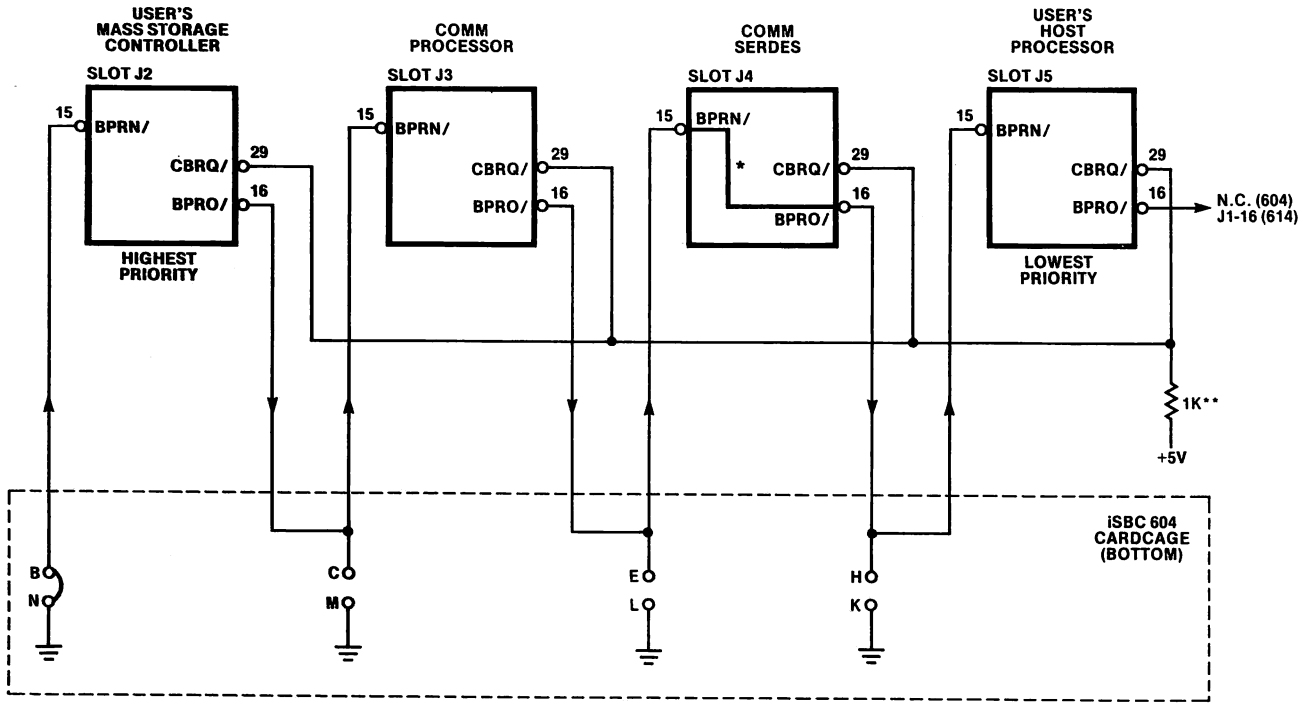
Before installing the controller, verify and/or reconfigure the switch setting and jumper placements on the processor board as described in the following paragraphs. (Refer to figure 2-3 for the location of the switch and plug-in jumpers.)

2-10. CONTROLLER WAKEUP I/O PORT ADDRESS SELECT

Controller wakeup by the host system processor is achieved by writing to one of the 12 jumper-selectable I/O ports listed in table 2-4. Notice in table 2-4 that either 8-bit or 16-bit host I/O addressing is accommodated.

2-11. INTERRUPT LEVEL SELECT

Host system processor wakeup by the controller can be assigned to any one of the eight interrupt priority levels (INT0/ - INT7) on the Multibus interface. The priority level is selectable by rotary INT LEVEL switch S1 as shown in table 2-5.



*SERDES BOARD CONNECTS PINS 15 AND 16 TOGETHER.

**REQUIRED ONLY IF CBRQ/ IS USED (SEE PARAGRAPH 2-14). PULL-UP RESISTOR IS SUPPLIED BY USER. ALL NON-CBRQ/ BUS MASTERS MUST HAVE HIGHER PRIORITY. IF NON-CBRQ/ DEVICE IS PLACED AT A LOWER PRIORITY, IT WILL NOT BE ABLE TO ACQUIRE THE BUS.

Figure 2-2. Serial Bus Priority Resolution Scheme 121746-3

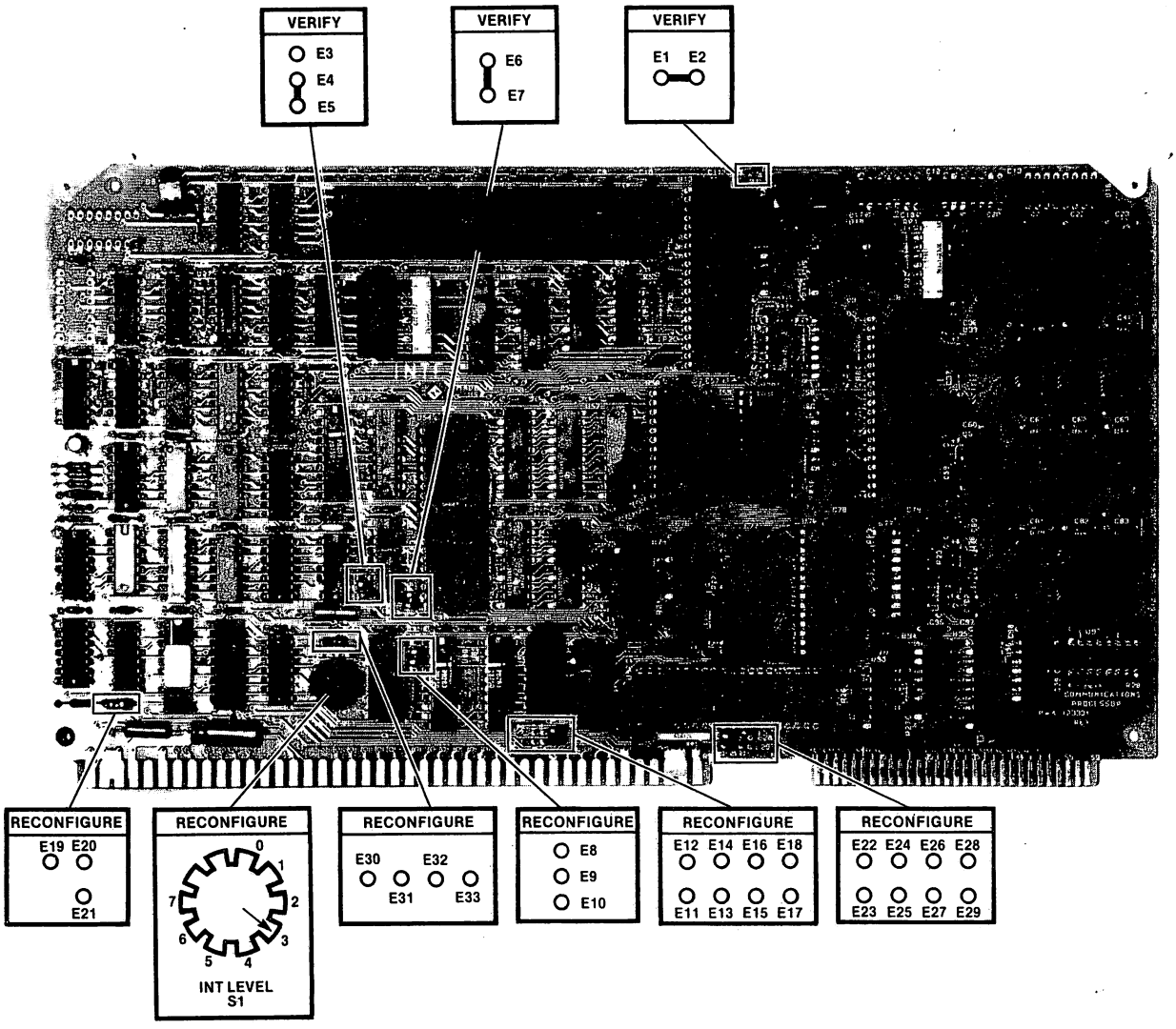


Figure 2-3. User-Configurable Switch and Jumpers

121746-4

Table 2-4. Controller Wakeup I/O Port Address Jumpers

Port Address	Plug-In Jumpers							
	E8-E9	E9-E10	E11-E12	E13-E14	E15-E16	E17-E18	E30-E31	E32-E33
A4H	IN	OUT	OUT	OUT	OUT	IN	Jumper may be installed in either E30-E31 or E32-E33	
A5H	IN	OUT	OUT	OUT	IN	OUT		
A6H	IN	OUT	OUT	IN	OUT	OUT		
A7H	IN	OUT	IN	OUT	OUT	OUT		
8A4H	OUT	IN	OUT	OUT	OUT	IN	OUT	IN
8A5H	OUT	IN	OUT	OUT	IN	OUT	OUT	IN
8A6H	OUT	IN	OUT	IN	OUT	OUT	OUT	IN
8A7H	OUT	IN	IN	OUT	OUT	OUT	OUT	IN
9A4H	OUT	IN	OUT	OUT	OUT	IN	IN	OUT
9A5H	OUT	IN	OUT	OUT	IN	OUT	IN	OUT
9A6H	OUT	IN	OUT	IN	OUT	OUT	IN	OUT
9A7H	OUT	IN	IN	OUT	OUT	OUT	IN	OUT

Table 2-5. Interrupt Priority Level Selection

S1 Switch Position	Interrupt Level	Priority
0	INT0/	Highest
1	INT1/	
2	INT2/	
3	INT3/	
4	INT4/	
5	INT5/	
6	INT6/	
7	INT7/	Lowest

2-12. COMMON BUS REQUEST SELECT

A plug-in jumper is provided to allow compatibility with user systems employing the Common Bus Request (CBRQ/) signal on the Multibus interface. (See tables 2-1 and 2-2.) Configure this jumper as follows:

E20-E21: CBRQ/ employed
E19-E20: CBRQ/ not employed

2-13. SYSTEM COMPATIBILITY SELECT

When in the reset, initialization, or bootstrap state, the command block address is fetched from a particular address in host system memory. The starting address in the communications system area is dependent upon which system is employed to host the controller. Because there is no unique memory location that the various Intel systems have in common, and to allow flexibility in the application of user-designed systems, plug-in jumpers are provided to accommodate a variety of system configurations. (Refer to table 2-6.)

Table 2-6. System Compatibility Selection Jumpers

Host System	Communications Area Starting Address	Plug-In Jumpers			
		E22-E23*	E24-E25	E26-E27	E28-E29
Series II/800	0F690H	OUT	IN	IN	IN
Series III (IPC)	0F690H	OUT	IN	IN	IN
Series III (RPB-86)	1F000H	OUT	IN	IN	OUT
Reserved	Reserved	OUT	IN	OUT	IN
User 1	1000H	OUT	IN	OUT	OUT
User 2	8000H	OUT	OUT	IN	IN
User 3	10000H	OUT	OUT	IN	OUT
User 4	20000H	OUT	OUT	OUT	IN
User 5	2F000H	OUT	OUT	OUT	OUT

*A jumper installed in E22-E23 will cause the firmware diagnostic to loop repeatedly on power-up or reset.

2-14. PROCESSOR/SERDES INTERFACE

The processor and SerDes boards communicate with one another through a 60-pin edge connector (P2). The P2 edge connectors are connected together through one of the two supplied dual auxiliary connectors. One dual auxiliary connector (Part No. 1000751) accommodates the Intel Series II, Series III, and iSBC 604/614 backplanes. The other dual auxiliary connector (Part No. 1000515) accommodates the Intel Model 800 backplane.

The dual auxiliary connector can optionally be mechanically fastened to the backplane. To mount the connector in the iSBC 604/614 Backplane, for example, proceed as follows:

WARNING

Always turn off system power and disconnect the power cord when accessing the interior of the cardcage.

a. Turn off system power and disconnect power cord.

b. From front (connector side) of backplane, position dual auxiliary connector over corresponding "A" connector (e.g., J2A and J3A) mounting holes.

c. Secure dual auxiliary connector in place using four 4-32 by 0.5 inch flathead screws, flat washers, and locking nuts. (Screws, washers, and locking nuts are not supplied.)

d. Reconnect power cord but do not turn on system power.

Figure 2-4 shows how to install the dual auxiliary connector when it is not mechanically fastened to the backplane. In this case, ensure that the dual auxiliary connector is properly aligned with the traces on the P2 edge connectors. Note in figure 2-4 that the dual auxiliary connector is installed such that the processor board will be mounted above the SerDes board when installed in the Series II, Series III, or iSBC 604/614 backplane. The positions of the two boards in the Series II and Series III systems can be reversed

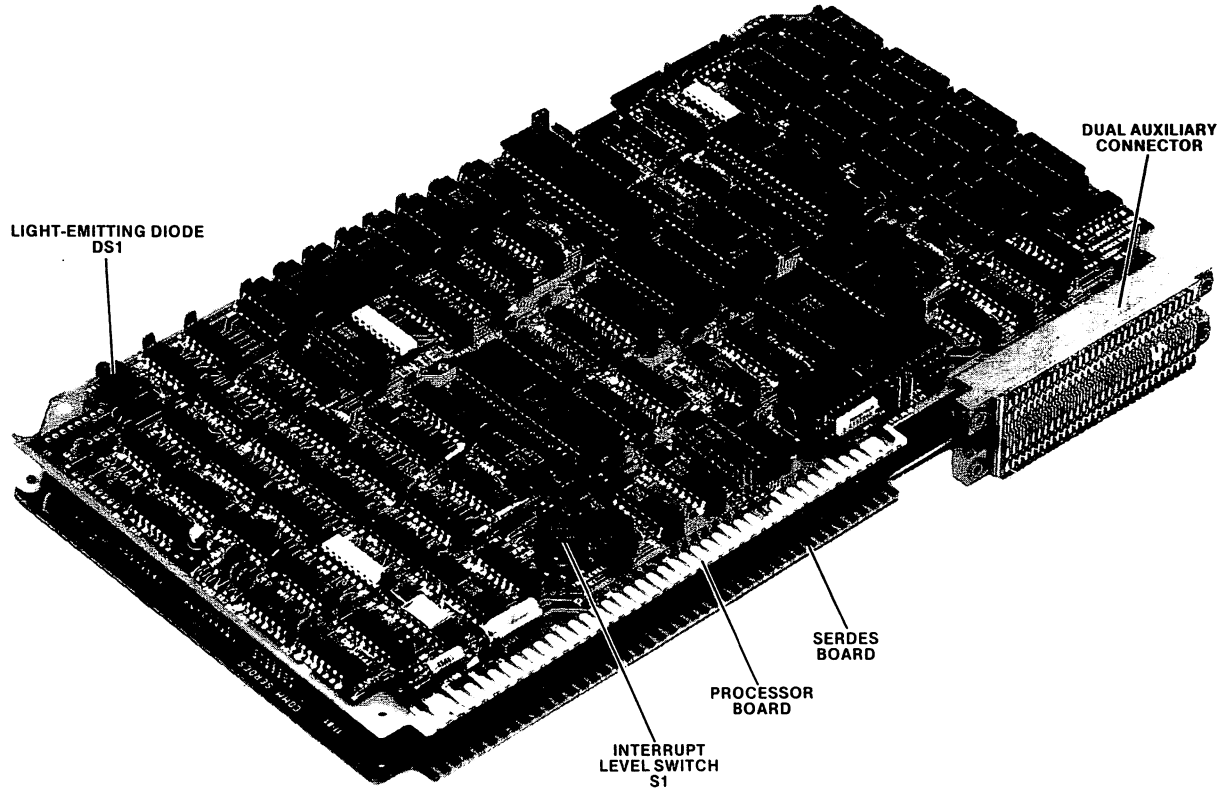


Figure 2-4. Processor/SerDes Board Interface 121746-5

(SerDes board above the processor board) without affecting their operation. In a Model 800 system, the only restriction is that the processor board must be installed in an odd-numbered slot. The position of the two boards in an iSBC 604/614 backplane depends upon the user implementation of the serial bus priority resolution scheme. (Refer to paragraph 2-8.)

2-15. BOARD INSTALLATION

CAUTION

To prevent possible equipment damage, do not install a board in or remove a board from the cardcage while power is applied to the chassis!

NOTE

Inspect the iSBC 604/614 Cardcage and ensure that pull-up resistors are installed for pins 28, 29, 30, 32, and 34. Earlier backplanes did not include these pull-up resistors.

The controller occupies two adjacent cardcage slots. It is recommended that the controller have a bus priority higher than the host processor but lower than the disk/diskette controller. (Refer to paragraph 2-8.) Table 2-7 lists the various cardcages together with their highest and lowest priority slots. After installing the controller, press firmly inward on all four extractor handles to seat both boards firmly into their mating backplane connectors.

Table 2-7. Bus Priority Vs. Cardcage Slot

System Cardcage	Highest Priority	Lowest Priority
Series II/III Model 800*	Bottom Slot Slot 17	Top Slot Slot 1
604/614	User Defined	
*Controller processor board must be installed in an odd-numbered slot.		

2-16. SERDES EXTERNAL INTERFACE

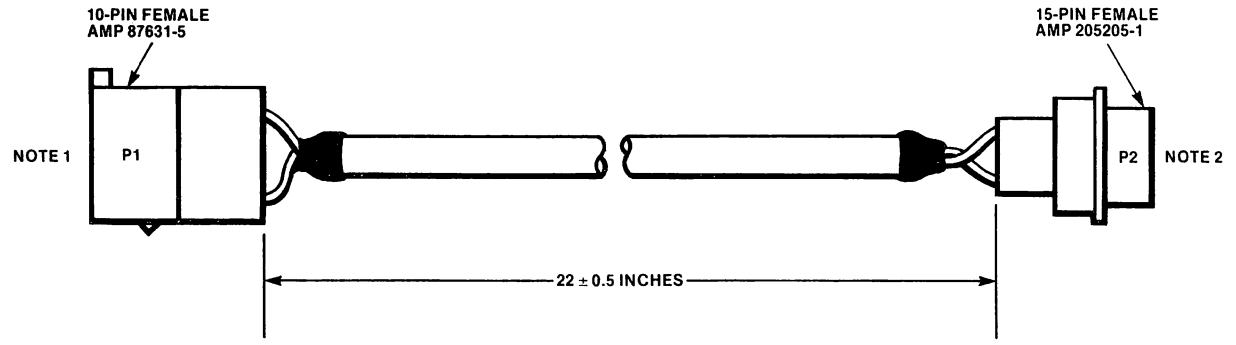
Details of the supplied internal transceiver cable (Part No. 123591) are given in table 2-8. The user must supply and connect the external transceiver cable, transceiver assembly, and coaxial cable as shown in figure 2-5. For specifications on the transceiver cable, transceiver, and coaxial cable, refer to *The Ethernet Data Link Layer and Physical Layer Specifications*, Version 1.0 (or later).

2-17. CONFIDENCE TEST

The firmware-resident confidence test, described briefly in Chapter 6 and in more detail in the *Ethernet Communications Controller Programmer's Reference Manual*, exercises the basic functions of the controller and illuminates a light-emitting diode (LED) on the processor board if the test fails. (See figure 2-4.) After the controller boards are installed and the SerDes board external connections are made to the coaxial cable, turn on the system power. If the LED remains unlighted, it can be assumed that the controller is operational.

The confidence test is normally executed only once on power-up or system reset. If it is desired to loop repeatedly on the confidence test, insert a plug-in jumper in position E22-E23. (Refer to paragraph 2-13 and figure 2-3.)

Table 2-8. Cable Assembly 123591 Details



P1 Pin Number	Function		P2 Pin Number
1	Transmit +	Twisted Pair	3
2	Transmit –		10
3	Receive +	Twisted Pair	5
4	Receive –		12
5	Collision +	Twisted Pair	2
6	Collision –		9
7	+12 Vdc Return	Twisted Pair	6
9	+12 Vdc		13

NOTES:

1. Mates with SerDes board connector J3 (see figure 2-5).
2. Mates with 15-pin male delta connector on user-supplied external transceiver cable (see figure 2-5.)
   Male delta connector part numbers:
   Shell: AMP 205206-1
   Crimp Contact: AMP 66506-4

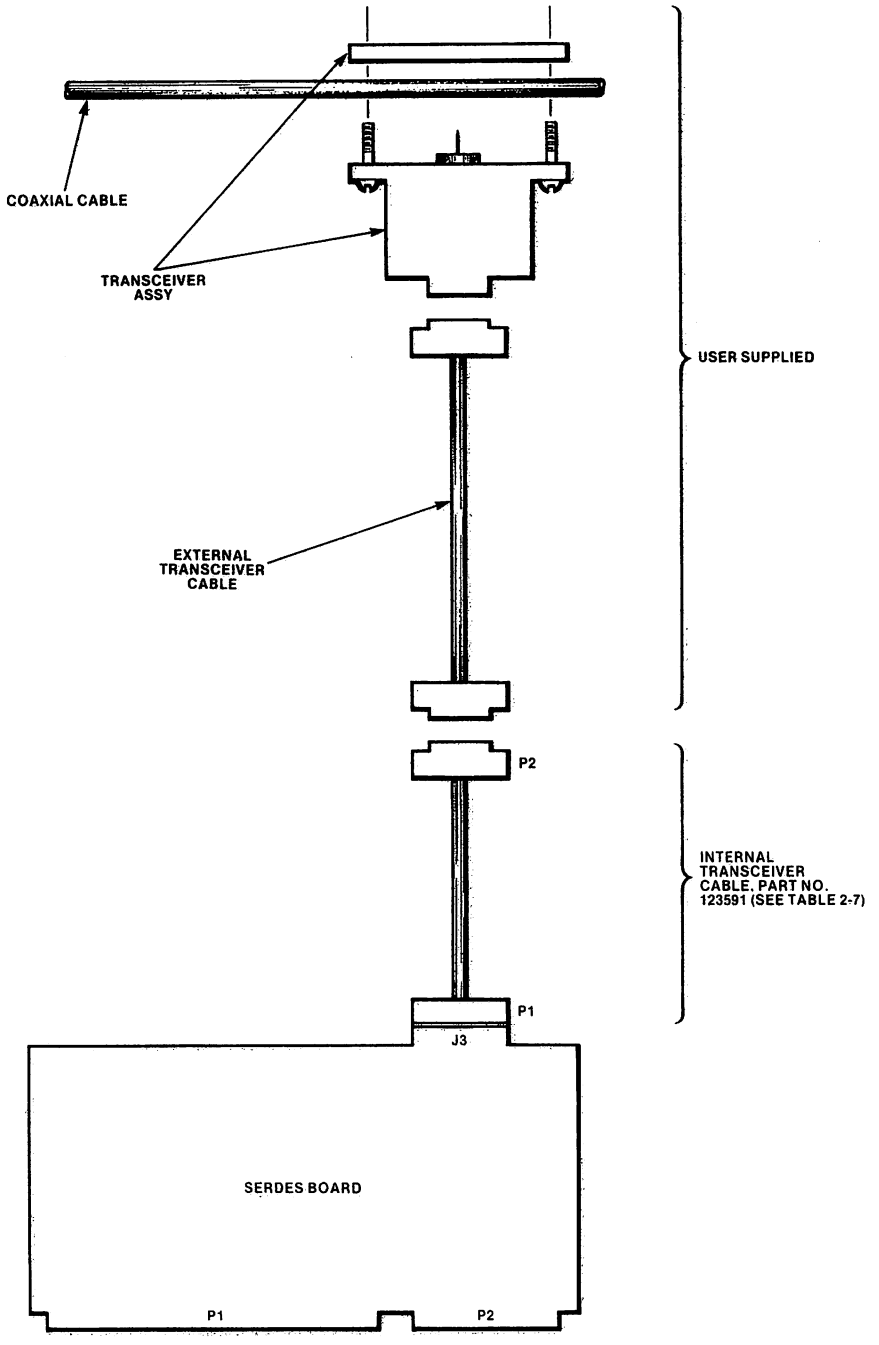
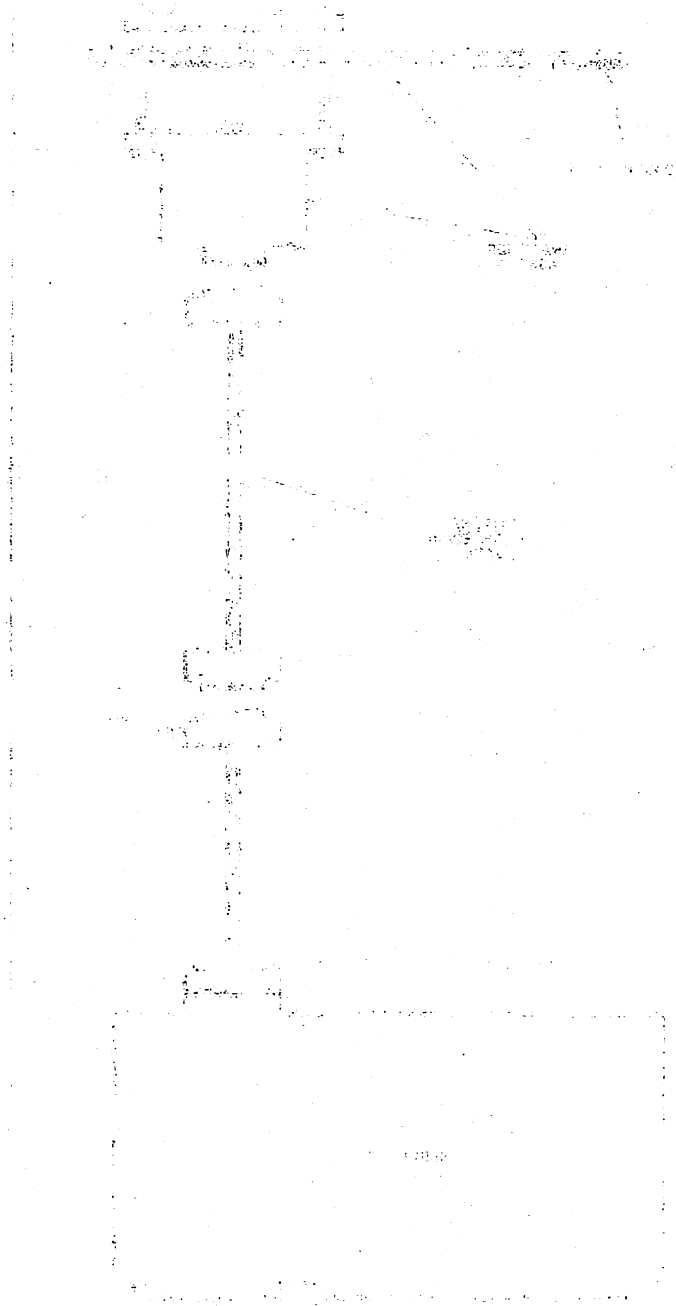


Figure 2-5. SerDes Board/Transceiver Interface

121746-6



CHAPTER 3
FUNCTIONAL OVERVIEW

3-1. INTRODUCTION

This chapter provides a functional overview of the processor board and SerDes board architecture and the associated transmit, receive, read address, and verify functions. Located at the end of this chapter are functional block diagrams of the processor board (figure 3-2) and the SerDes board (figure 3-3).

3-2 PROCESSOR BOARD ARCHITECTURE

The architecture of the processor board is based on the local bus, DMA bus, and the interface to the Multibus™ (system bus). The primary function of the processor board, which includes an 8088 Microprocessor, is buffering, processing, and transferring processed data packets to and from system memory. The processor board includes the capabilities of generating an interrupt to the host system processor and accessing system memory and I/O devices. It also includes an I/O port that allows the reception of a command interrupt (wakeup), reset interrupt command, and a hardware reset command from the host system processor.

Located on the local bus are the 16k Dynamic RAM memory (DRAM), 8202 Dynamic RAM Controller, 8k read-only memory (ROM), 8253 Programmable Interval Timer (PIT), 8255A Programmable Peripheral Interface (PPI), and 8259A Programmable Interrupt Controller (PIC). The local bus memory and I/O devices play the following roles in the overall communications process:

a. 16k DRAM Memory. Used primarily for storage of code downloaded from the system and executed by the 8088 CPU.

b. 8k ROM Memory. Contains the Data Link Layer (DLL), External Data Link (EDL), Multibus Interprocessor Protocol (MIP), bootstrap, and power-up confidence test firmware.

c. 8253 PIT. Includes the following three timers:
   1. Alarm Clock (Timer 0)—Wakes up 8088 CPU after a program halt.
   2. Real-Time Clock (Timer 1)—Provides timing mark for time-of-day software.
   3. Backoff Timer (Timer 2)—Executes binary exponential backoff algorithm used in collision avoidance.

d. 8255A PPI. Includes the following three ports:
   1. Port A (Input)—Allows 8088 CPU to read status of system interrupt, DMA bus, and SerDes board.
   2. Port B (Output)—Allows 8088 CPU to control various SerDes board functions.
   3. Port C (Input/Output)—Upper four bits (output) used to lock system bus, verify transceiver, and drive confidence test light-emitting diode. Lower four bits (input) are programmable by plug-in jumpers to select compatible host system processor command block address.

e. 8259A PIC. Handles eight interrupt requests to 8088 CPU in a positional rotating scheme. Interrupt sources are from the four 8237-2 DMA channels (three receive, one transmit), the three 8253 PIT timers, and the host system processor.

Located on the DMA bus is a discrete Bus Arbiter, 8k static RAM memory (SRAM), and an 8237-2 Programmable DMA Controller. The 8k SRAM memory is used as a buffer for data being transferred to and received from the SerDes board. The 8237-2 includes four channels. Due to hardware restrictions, channel 0 is dedicated to the transmit sequence and channels 1, 2, and 3 to receive sequences. The three receive channels operate in a rotating mode so that back-to-back data packets from the serial link may be transferred at maximum speed into SRAM memory. (The DMA receive channel sequencer is located on the local bus.) The discrete Bus Arbiter resolves contention between the 8088 CPU and 8237-2 DMA Controller for control of the DMA bus.

The theory of operation describing the timing and logic involved in implementing the processor board functions is provided in Chapter 4.

3-3. SERDES BOARD ARCHITECTURE

The SerDes board architecture is composed primarily of ECL and TTL components. Included on the SerDes board are the transceiver interface, channel clock, channel data encoder and decoder, preamble generator, station address generator and recognizer, CRC generator and checker, and carrier sense and collision detect circuits. These circuits provide the

following physical channel receive and transmit functions:

a. Generating the clocks for synchronization and timing.

b. Performing serial-to-parallel and parallel-to-serial conversion of data to and from the processor board.

c. Transmitting and receiving serial bit streams via the transceiver interface.

d. Detecting a carrier (non-idle channel).

e. Detecting a collision (simultaneous transmission attempt by two or more stations).

f. Translating the clock and data into a single, self-synchronizable serial bit stream suitable for transmission.

g. Decoding to separate the incoming phase-encoded bit stream into a data stream and a clock signal.

h. Generating and inserting the preamble, which is used for synchronization at the receiving site, before the first data byte in each transmit frame. (Refer to paragraph 3-4.)

i. Generating and recognizing the station's 48-bit address.

j. Generating and appending a frame check sequence (FCS) field to each transmit frame to allow the detection of transmission errors. The FCS field is a 32-bit cyclic redundancy check (CRC) code.

The theory of operation describing the timing and logic involved in executing these functions is provided in Chapter 5.

3-4. FRAME FORMAT

Figure 3-1 illustrates the preamble and the five fields comprising a frame: destination address, source address, type, data, and frame check sequence. All five fields are of fixed size except the data field, which may range from 46 bytes minimum to 1500 bytes maximum. The order of transmission is from left to right; i.e., the preamble is transmitted first and the frame check sequence is transmitted last.

3-5. DESTINATION ADDRESS FIELD

The 48-bit (6-byte) destination address, which specifies the station(s) for which the frame is intended, is one of two types: physical or multicast. A physical address is assigned to one (and only one) station in the net; a multicast address is associated with two or more stations in the net. There are two types of multicast addresses:

a. Group address—an address associated by a higher-level convention with a group of logically related stations.

b. Broadcast address—a predefined address that denotes all stations in the net.

PREAMBLE	DEST ADDR	SRC ADDR	TYPE	DATA	FCS
64	48	48	16	(46 to 1500) x 8	32

PREAMBLE: 62 BITS OF ALTERNATE 1's AND 0's FOLLOWED BY TWO CONSECUTIVE 1's

DESTINATION ADDRESS: 48 BITS;
1ST BIT = 0 = PHYSICAL ADDRESS
1ST BIT = 1 = MULTICAST ADDRESS

SOURCE ADDRESS: PHYSICAL ADDRESS ONLY

TYPE: RESERVED FOR HIGHER LEVEL

DATA: 46 TO 1500 BYTES

FCS: $P(X) = X32 + X26 + X23 + X22 + X16 + X12 + X11 + X10 + X8 + X7 + X5 + X4 + X2 + X + 1$

Figure 3-1. Frame Format 121746-7

The first bit of the destination address field distinguishes between physical and multicast addresses: 0 = physical address and 1 = multicast address. In either case, the remainder of the first byte and the subsequent five bytes form a 47-bit pattern. In the case of a broadcast address, the pattern consists of 47 one's.

3-6. SOURCE ADDRESS FIELD

The 48-bit (6-byte) source address field identifies the station sending the frame.

3-7. TYPE FIELD

The 16-bit (2-byte) type field is reserved for use by higher levels.

3-8. DATA FIELD

The data field must consist of at least 46 bytes and not more than 1500 bytes.

3-9. FRAME CHECK SEQUENCE FIELD

The frame check sequence (FCS) field contains a 32-bit (4-byte) cyclic redundancy check (CRC) value. This value is computed by the SerDes board as a function of the contents of the destination address, source address, type, and data fields.

3-10. FRAME SIZE LIMITATIONS

Given the minimum and maximum size of the data field and the total 18 bytes of the other four fields, the smallest valid frame contains 64 bytes and the largest valid frame contains 1518 bytes.

3-11. OPERATIONS SEQUENCES

The functions performed by the SerDes board are transmit, receive, read address, and verify sequences. These sequences are selected by the set of programmable control signals listed in table 3-1. These signals, with the exception of TXSRT, are output to the SerDes board by the 8255A PPI; TXSRT is set and cleared through a discrete latch.

3-12. TRANSMIT SEQUENCE

After assembling a frame in SRAM memory, the Data Link Layer (DLL) firmware initializes DMA channel 0 with the word count and the base address. (The word count is equal to the total number of bytes in the destination address, source address, type, and data fields; the base address points to the first byte of the frame in SRAM memory.) The DLL firmware then sets the necessary control bits in the 8255A (Port B) and outputs the Transmit Start (TXSRT) control signal to the SerDes board.

The SerDes board continuously monitors the data link and, when TXSRT goes true, will not start a transmission unless the data link has been quiet for a minimum of 9600 nanoseconds (96 bit times). If a transmission is currently in progress or the data link

Table 3-1. SerDes Board Sequence Control Signals

Signal	Transmit	Receive	Read Address	Verify Onboard	Verify Transceiver
CLR SER	0	0	0	0	0
READ ADD/	1	1	0	1	1
FRC CRC	1/0	X	0	0	0
PROMISCUOUS RCV/	X	1/0	0	1	1
NORMAL MODE	X	1/0	1	0	0
VERIFY ON BRD/	1	1	1	0	1
RXEN/	X	0	1	0	0
TXEN/	0	X	1	0	0
VERIFY XCVR/	1	1	1	1	0
TXSRT	1	X	0	1	1

1 = High
0 = Low
X = Don't Care
1/0 = Programmable

has not been quiet for 9600 nanoseconds, the SerDes will defer the start of the transmit sequence. When the data link is deemed clear, the SerDes board asserts the Transmit Request (TXRQ) signal to DMA channel 0 to begin DMA bus arbitration and to start the frame transfer.

As shown in figure 3-1, the transmit data stream consists of a serialized preamble and the five fields of the frame. The SerDes board hardware automatically inserts the preamble ahead of the frame before transmitting the first bit of the destination address field. (The first bit of the destination address field is the least-significant bit of the first byte fetched from SRAM memory.) After serializing and transmitting the first four fields, the SerDes board appends the computed FCS field.

When the transmit sequence is completed, the SerDes board asserts the Transmit Complete (TXC) signal, which generates an interrupt request to 8088 CPU via the 8259A PIC. There are three conditions under which the SerDes board will terminate the transmission:

a. Normal Termination: Preamble and frame transmitted properly; no status bit set.

b. Transmit Time Out: Time required to transmit the combined preamble and frame exceeded 3.5 milliseconds. SerDes board will abort the transmission and set the Transmit Time Out (TXTO) status bit.

c. Transmit Collision: SerDes board detected a collision; i.e., another station attempted simultaneous transmission. SerDes board will then transmit an additional 32 to 48 zeroes for collision reinforcement, terminate the transmission, and set the Transmission Collision (TX CLSN) status bit.

When the 8088 CPU detects that a collision has occurred (TX CLSN status bit set), it clears TXSRT and begins executing a backoff algorithm by loading a count into counter 2 of the 8253 PIT. After the 8253 reaches the terminal count and interrupts the 8088 CPU via the 8259A PIC, the 8088 CPU once again intiates the transmit sequence.

3-13. RECEIVE SEQUENCE

Prior to a receive sequence, the enabled DMA receive channel is initialized with the base address and a word count of 1521 (largest valid frame size plus three bytes for startup and shutdown purposes). The SerDes board continuously monitors the data link and, if the PROMISCUOUS RCV/ signal is true, will ensure the reception of *all* data packets regardless of the destination address field. If the PROMISCUOUS RCV/ signal is false, the SerDes board will examine the destination address field of each data packet and either receive or ignore the packet as follows:

a. If first bit = 1, signifying a broadcast or multicast address, data packet will be received.

b. If first bit = 0, signifying a physical address, all 48 bits will be compared to onboard station address.

If the destination address does not match, a premature shutdown of the receive logic occurs and no indication of such action is reported to the processor board. If the destination address matches, the SerDes board generates the proper control and status signals to initiate the DMA transfer of data into the SRAM memory. The receive sequence continues until one of the following ending conditions occurs:

a. Activity on Receive Data line ceases, indicating end of data packet. If there is no CRC error, SerDes board generates a unique interrupt request (depending on which DMA receive channel was used) to 8088 CPU. If there is a CRC error, SerDes board will set CRC ERR status bit but no interrupt request to 8088 CPU will be made.

b. Participating DMA receive channel notifies SerDes board that data packet exceeds maximum allowable length. SerDes board will set LEN ERR status bit but no interrupt request to 8088 CPU will be made.

3-14. READ ADDRESS SEQUENCE

The 48-bit station address for the communications controller is contained in PROM on the SerDes board. The read address sequence is executed in order to store the station address in SRAM for later assembly into a transmit frame. Prior to issuing the READ ADD/ command, the appropriate DMA receive channel must be initialized with the base address and a word count of 18 bytes (2 invalid bytes plus 16 address bytes).

When the READ ADD/ command is asserted while the other SerDes control signals are in the states shown in table 3-1, the enabled DMA receive channel automatically transfers the 6-byte station address, eight bytes of zeros, and a 2-byte CRC into SRAM memory. After the last byte is transferred into SRAM memory, the SERDES board sets the LEN ERR status and asserts the Receive Complete (RXCMP) signal, which generates an interrupt request to the 8088 CPU. The reception of subsequent data packets will be inhibited until LEN ERR is cleared by the Reset Error command and the SerDes board is reset.

3-15. VERIFY ONBOARD SEQUENCE

The verify onboard sequence is part of the firmware-resident confidence test that verifies the operation of all SerDes board data flow and control logic except the transceiver driver interface. The SerDes board may be assumed to be operational if all transmit and receive status signals are as expected after the sequence is completed.

With the control bits set as given in table 3-1, the SerDes board will begin the verify onboard sequence when the TXSRT control signal goes true. This sequence is the same as a transmit sequence and a receive sequence operating simultaneously except as follows:

a. FCS field is not automatically computed and appended as part of transmit packet by CRC generator; FCS field is part of test transmit packet stored in SRAM memory prior to TXSRT signal going true.

b. Received packet is not stored in SRAM memory due to bandwidth limitations.

3-16. VERIFY TRANSCEIVER SEQUENCE

The verify transceiver sequence, which is also part of the firmware-resident confidence test, is intended to be used after the operability of the SerDes board has been proven by the verify onboard sequence. Successful completion of the verify transceiver sequence assures proper operation of the transceiver cable connections and transceiver operation.

With the control bits set as given in table 3-1, the SerDes board will begin the verify transceiver sequence when the TXSRT control signal goes true. This sequence exercises the SerDes board circuits in much the same way as the verify onboard sequence. However, the transmit data in this test is routed through the transmit data pair to the transceiver and loops back to the SerDes board through the receive data pair.

CHAPTER 4
PROCESSOR BOARD THEORY OF OPERATION

4-1. INTRODUCTION

The communication processor board schematic diagram is provided in figure 6-1 (11 sheets). Signals that traverse from one sheet to another are identified by an alphabetic character(s) in a box (e.g., [A], [CE], etc.). Adjacent to each such box are the signal name and the grid coordinates of the signal source or destination. For example, the grid coordinates 2D8 locate a signal source (or signal destination as the case may be) on sheet 2 in zone D8.

Both active-high and active-low signals are used. A signal mnemonic that ends with a slash (e.g., DAT7/) denotes that the signal is active low ($\leq$0.4V). Conversely, a signal mnemonic without a slash (e.g., ALE) denotes that the signal is active high ($\geq$2.0V).

Described in following paragraphs are the logic and timing details involved in executing the overall functions of the processor board.

4-2. PROCESSOR RESET

When power is initially applied to the processor board, the contents of LSI circuit registers and discrete latches are subject to random factors and cannot be predicted. For this reason, a power-on hardware reset is used to guarantee certain circuits to be in a known initial state.

Upon the application of power, capacitor C89 (4D7) begins to charge through resistor R24. The charge developed across C89 is sensed by a Schmitt trigger internal to the 8284A Clock Generator/Driver, which converts the input appearing at pin 11 into a clean, fast-rising RESET output signal at pin 10. This signal is gated through U49-10 and U26-8 to the 8088 CPU (sheet 4), 8255A Programmable Peripheral Interface (sheet 6), 8237-2 DMA Controller (sheet 11), Multibus Interrupt (MB INT) latch (sheet 3), System/Local (SYS/LOC) bus latch (sheet 5), and the Multibus I/O Enable (MBUSIOEN) latch (sheet 8). The RESET signal performs the following:

a. Clears the 8255A control register and sets all three ports to the input mode.

b. Clears the 8237-2 internal registers and sets it to the inactive (idle) cycle.

c. Clears MB INT latch U69-5, MBUSIOEN latch U36-5, and SYS/LOC bus latch U27-9.

d. Causes the 8088 CPU to fetch and execute the contents of location FFFF0H, which is the entry point to the firmware power-up diagnostic module.

The same hardware functions can also be initiated by means of the system bus INIT/ signal applied through gate U43-8 (2D1), or by the system host processor software. The INIT/ signal, which is generated by the system host processor when power is initially applied or when the system front panel RESET switch is pressed, also initializes the 8289 Bus Arbiter (2D1), causing it to three-state (float) its outputs to prevent system bus contention problems during system power up. The system host processor can also reset the processor board by means of an I/O write instruction as described in paragraph 4-16.

4-3. CLOCK CIRCUITS

References for most on-board timing functions are provided by the 8284A Clock Generator (4D6) in conjunction with crystal Y2. The 8284A divides the 15-MHz fundamental crystal frequency to produce the 5-MHz CLK, CLKB, and CLK/ signals as well as the 2.5-MHz PCLK signal. The timing reference for the 8202A Dynamic RAM Controller (8C5) is provided by a 20-MHz crystal (Y1).

The 8284A Clock Generator also supplies the READY signal to the 8088 CPU. The 8284A asserts READY on the next positive-going edge of CLK after the Multibus Ready (MB RDY) or On Board Ready (ON BD RDY) signal is asserted by the addressed on-board or system bus device.

4-4. 8088 CPU TIMING

The 8088 CPU is responsible for executing the resident firmware and software as well as transferring data between the processor board and the system bus. The CPU uses the CLK signal to develop the overall timing requirements for the various time-dependent functions described in the following paragraphs. Detailed timing and related internal CPU functions are described in *The 8086 Famly User's Manual*, Order No. 9800722.

4-5. BASIC TIMING

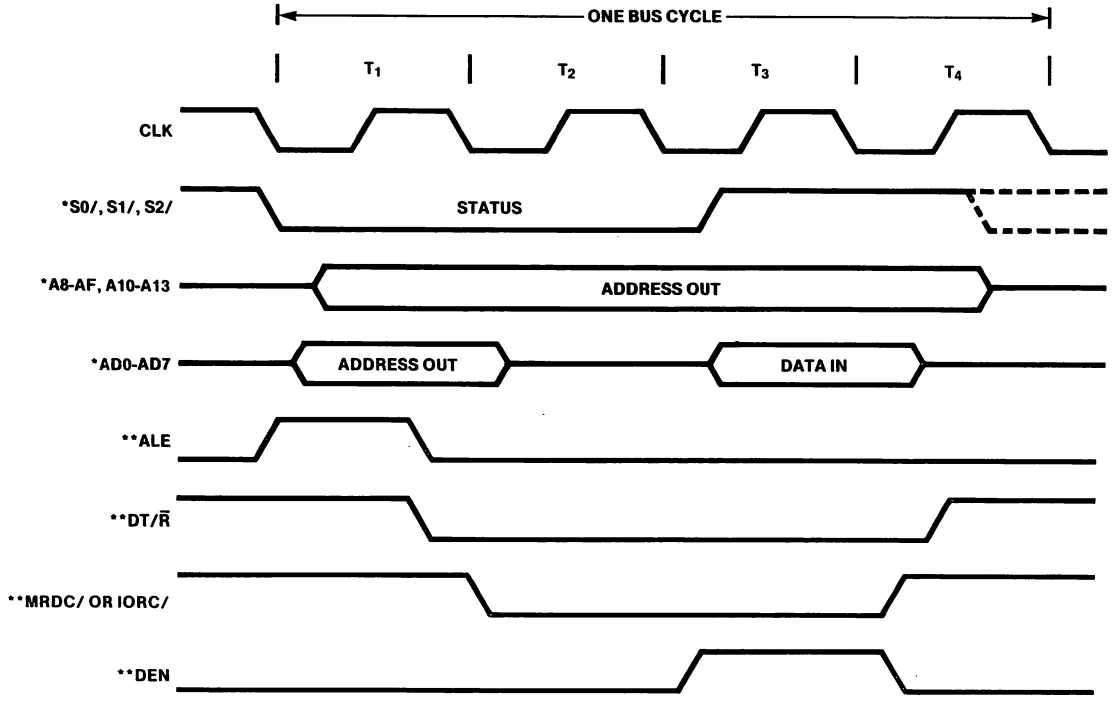
Each CPU bus cycle consists of at least four clock (CLK) periods referred to as states T_1, T_2, T_3, and T_4. The CPU places the memory or I/O device address on the bus during state T_1. During a write cycle, the CPU places data on the bus from state T_2 until state T_4. During a read cycle, the CPU accepts data on the bus from state T_3 until state T_4. During a read or write cycle, state T_2 is used primarily for changing the direction of the multiplexed address/data bus. In the event that the addressed memory or I/O device does not respond immediately to the read or write command, the CPU inserts wait (T_W) states between T_3 and T_4. Each T_W state is the same duration as one clock period. Clock periods during which there is no CPU-driven bus activity are called idle (T_I) states. Typically, the CPU inserts idle states while executing a lengthy instruction.

4-6. BUS TIMING

At the beginning of state T_1 in every bus cycle, the CPU activates status signals S0/, S1/, and S2/. These status signals are decoded by the enabled 8288 Bus Controller (2D6 and 4B4) and the 8289 Bus Arbiter (2D4) to identify the following CPU cycles:

Status Signal			CPU Cycle
S2/	S1/	S0/	
0	0	0	Interrupt Acknowledge
0	0	1	I/O Read
0	1	0	I/O Write
0	1	1	Halt
1	0	0	Code Access
1	0	1	Memory Read
1	1	0	Memory Write
1	1	1	Passive

A memory or I/O read cycle begins in state T_1 with the CPU activating status signals S0/, S1/, and S2/, and placing the 20-bit address on the bus. (Refer to figure 4-1.) The trailing edge of the Address Latch Enable (ALE) signal, which is asserted by the enabled 8288 Bus Controller (U85 or U73) during T_1 of each CPU bus cycle, strobes the 20-bit address into address latches U52, U88, U89 (sheet 2) and U53,



*DENOTES CPU INPUT OR OUTPUT
**DENOTES ENABLED BUS CONTROLLER OUTPUT

Figure 4-1. CPU Read Cycle Timing 121746-10

U55, U71 (sheet 4). The enabled 8288 Bus Controller drives the Data Transmit/Receive (DT/$\overline{R}$) signal low toward the end of state T_1 to set up the various transceivers (data buffers) for inputting data to the CPU. Depending on whether it is a memory or I/O read cycle, the enabled 8288 Bus Controller asserts a Read Command (MRDC/) or I/O Read Command (IORC/) from the beginning of T_2 until the beginning of T_4. At the beginning of T_3, the CPU switches its multiplexed AD0-AD7 lines to the data mode and the enabled 8288 Bus Controller asserts the Data Enable (DEN) signal. (The DEN signal enables the transceivers, completing the data path to the CPU input.) During the last half of T_3, the CPU examines the state of its READY input to ascertain whether or not the addressed device has placed data on the bus. If READY is high, the CPU proceeds into T_4; if READY is low, the CPU becomes inactive for an integral number of wait (T_W) states until READY goes high. The external effect of using the READY signal is to preserve the exact state of the CPU at the end of T_3. This "stretching" of the system timing allows the CPU to accommodate memory and I/O devices having different access times; that is, by inserting T_W states, the CPU can read and write to slower memory or slower I/O devices. During T_4, the CPU accepts the data and terminates the command (MRDC/ or IORC/); the DEN signal then goes false and disables the data buffers.

A write cycle begins in state T_1 exactly as does a read cycle except for the DT/$\overline{R}$ signal; DT/$\overline{R}$ remains high throughout the read cycle to set up various transceivers (data buffers) for outputting data from the CPU. As shown in figure 4-2, 8288 Bus Controller U73 provides Advanced Memory Write (AMWC/) and Advanced I/O Write (AIOWC/) commands for the on-board RAM memory and I/O devices. These advanced write commands (strobes) are issued one state earlier than the normal Memory Write (MWTC/) and I/O Write (IOWC/) commands provided by 8288 Bus Controller U85. At the beginning of state T_2 in the write cycle, the CPU places the data on the bus and 8288 Bus Controller U73 asserts the AMWC/ or AIOWC/ command together with the DEN signal. (The DEN signal enables the data buffers, completing the data path from the CPU to the addressed device.) At the beginning of state T_3,

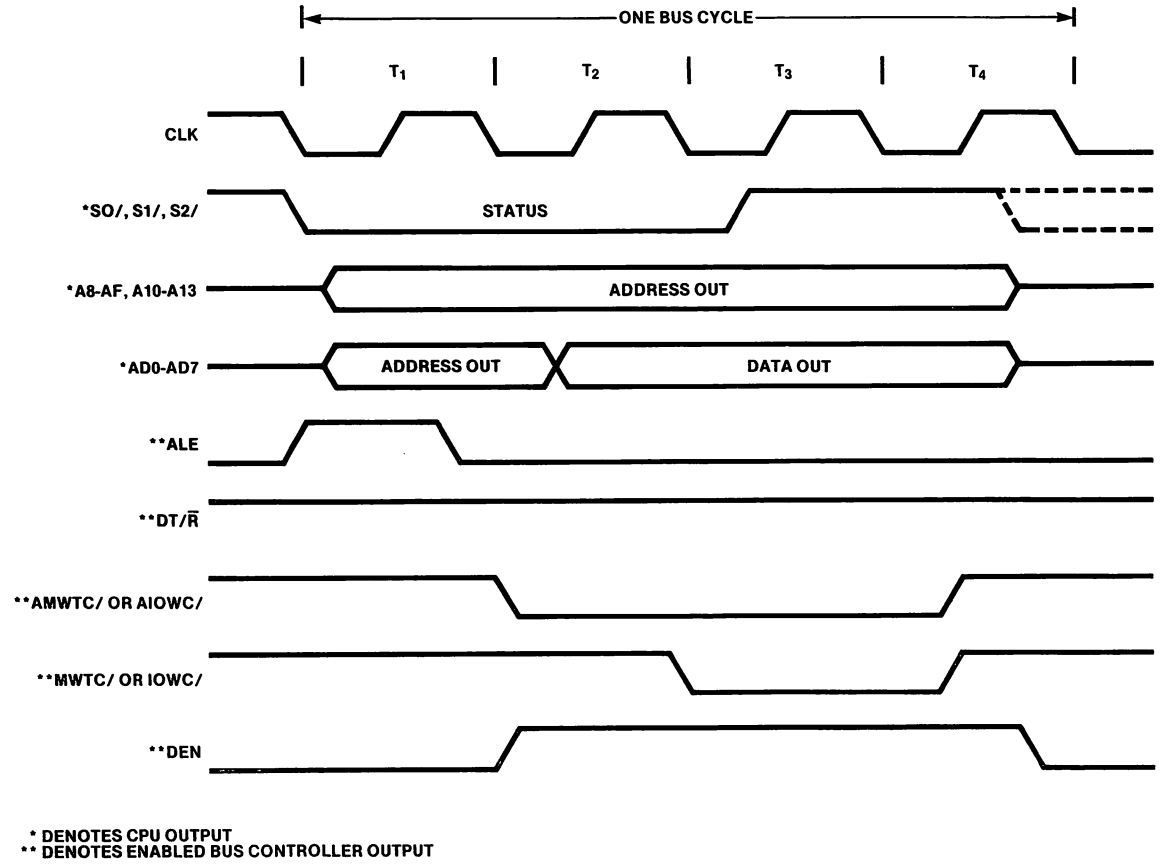


Figure 4-2. CPU Write Cycle Timing

121746-11

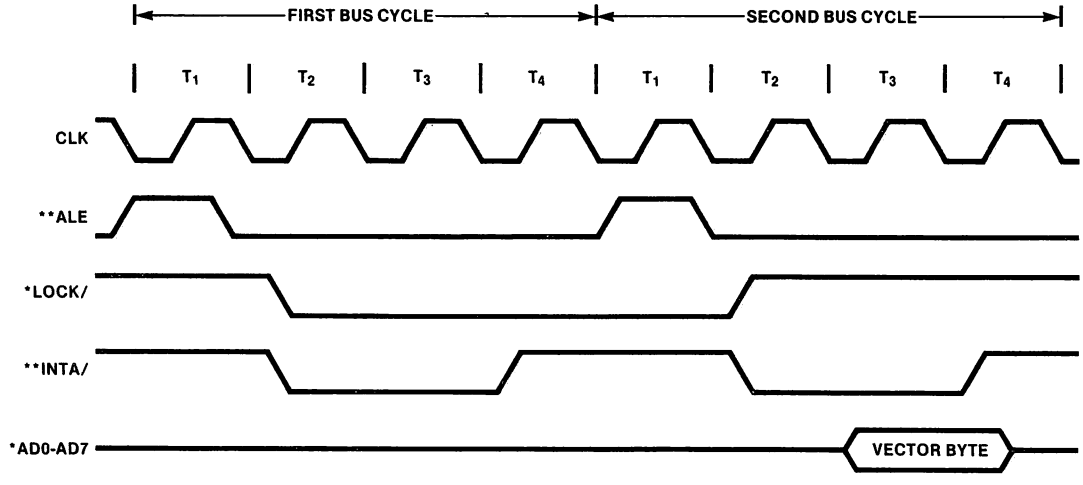
8288 Bus Controller U85 asserts the MWTC/ or IOWC/ command required for system bus operations. The CPU examines the state of its READY input during the last half of state T_3. When READY goes high (signifying that the addressed device has accepted the data), the CPU enters state T_4 and terminates the command. DEN then goes false and disables the data buffers.

Timing for the CPU interrupt acknowledge sequence is shown in figure 4-3. Two back-to-back interrupt acknowledge bus cycles are executed for each interrupt request (INTR) generated by the 8259A Programmable Interrupt Controller (7D5). When the 8259A drives its INTR output high, the CPU floats its address/data lines and activates the INTA/ command during states T_2 and T_3. (Note that the CPU also activates the LOCK/ command from state T_2 of the first bus cycle until state T_2 of the second bus cycle to prevent 8289 Bus Arbiter U84 from surrendering control of the system bus.) During the second bus cycle, the CPU again activates the INTA/ command and the 8259A responds by placing a data byte on the bus to identify the interrupt source. The CPU reads this byte, multiplies it by four, and uses the resultant value as a pointer to an interrupt vector table.

4-7. MEMORY ADDRESS MAPPING

In a memory read or write cycle, the address generated by the CPU will cause the hardware to enforce the memory address mapping shown in figure 4-4. There are three types of memory located on the processor board: dynamic RAM (DRAM), static RAM (SRAM), and read-only memory (ROM).

The 16k bytes of DRAM memory on the local bus are used primarily for storage of code downloaded from the system and executed by the 8088 CPU. Note in figure 4-4 that the 8088 CPU interrupt vector table resides in the lower 2k byte block 00000H-007FFH, which is the same *physical* block as F0000H-F07FFH. Because the 8088 CPU may also need to access the lower 2k bytes in system memory, an output I/O port control signal (SYS/LOC) is provided to allow the selection of the lower 2k bytes in system memory or the lower 2k bytes in local memory. (The 8088 CPU has free access to locations 00800H-EFFFFH in system memory.) As described in paragraphs 4-8 and 4-9, the SYS/LOC signal is controlled by writing to onboard I/O ports A0H and B0H. Since the interrupt vector table requires only 32 bytes (00000H-0001FH), the remaining 2016 bytes



*CPU OUTPUTS LOCK/, INPUTS AD0-AD7
**DENOTES ENABLED BUS CONTROLLER OUTPUT

Figure 4-3. CPU Interrupt Acknowledge Cycle Timing

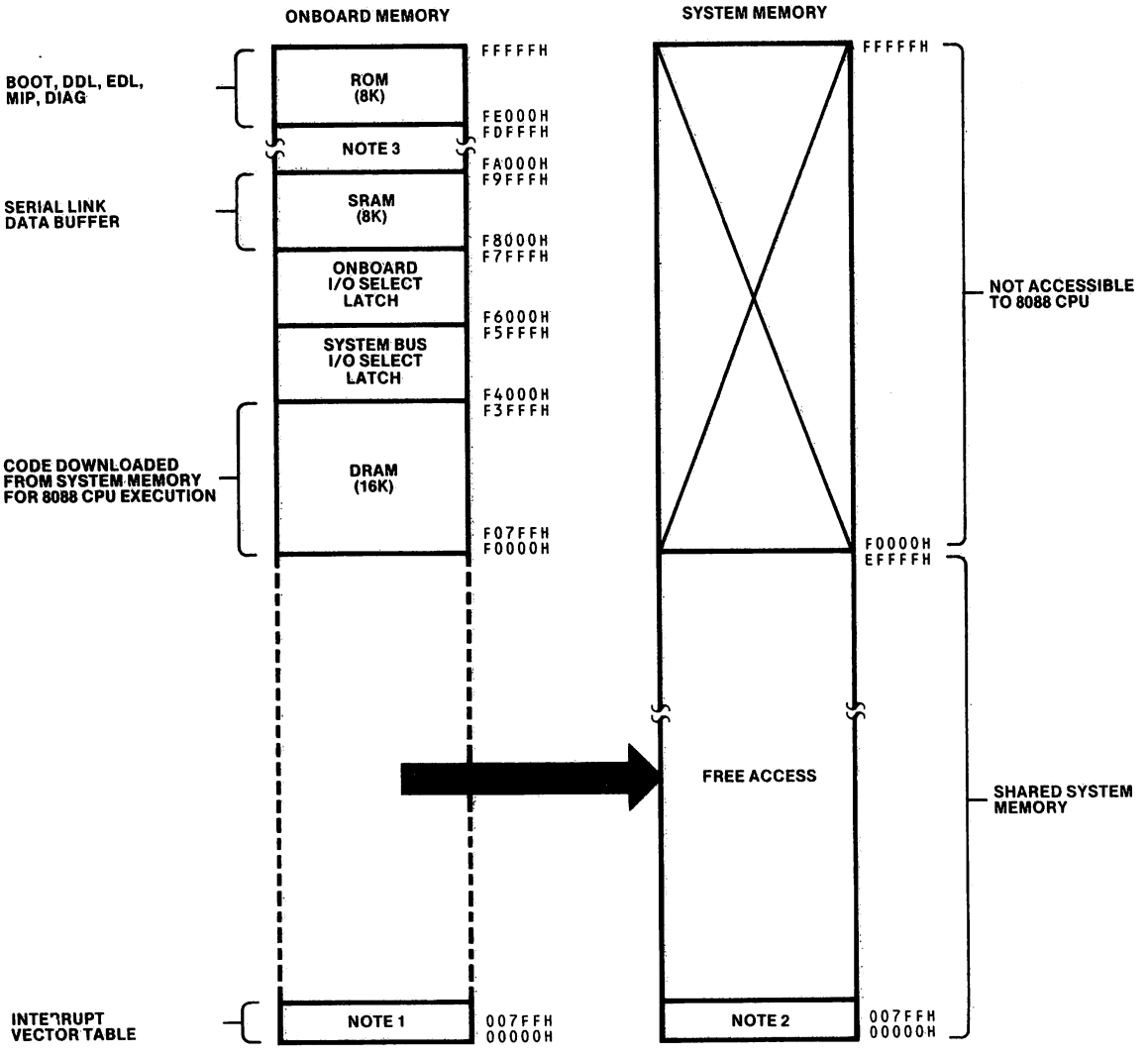
121746-12

can be used for program data storage and retrieval purposes. The DRAM memory imposes a maximum of five CPU wait (T_W) states and a minimum of one wait state for access.

The 8k bytes of SRAM memory on the DMA bus are used as a buffer for data being transferred to or received from the SerDes board. The SRAM memory imposes no CPU wait (T_W) states for access, thereby allowing a maximum DMA transfer rate of 1.25 megabytes per second.

The 8k bytes of non-volatile ROM memory on the local bus contain the following firmware modules: Data Link Layer (DLL), External Data Link (EDL), Multibus Interprocessor Protocol (MIP) implementation, bootstrap routine, and power-up/reset confidence test. The ROM memory imposes a maximum of one CPU wait (T_W) state for access.

Notice in figure 4-4 that onboard locations FA000H-FDFFFH are non-existent memory, and any attempt to read from this area will be meaningless.



NOTES:

1. SAME PHYSICAL DRAM AS F0000H-F07FFH. ACCESSED ONLY WHEN OUTPUT PORT CONTROL SIGNAL SYS/LOC = 0 (SEE TABLE 4-1).
2. ACCESSED ONLY WHEN OUTPUT PORT CONTROL SIGNAL SYS/LOC = 1 (SEE TABLE 4-1).
3. NON-EXISTENT MEMORY.

Figure 4-4. Memory Address Mapping 121746-13

4-8. SYS/LOC GENERATION

As described in the preceding paragraph, the SYS/LOC signal controls the access to the lower 2k bytes of CPU adressable memory or the lower 2k bytes of system memory. To access the lower 2k bytes of CPU addressable memory, the CPU executes an I/O write to onboard port B0H. The Advanced I/O Write (AIOW/) signal from 8288 Bus Controller U73 together with address bits ADD6-ADD7 enable binary decoder U34 (5C5). When enabled, U34 decodes address bits ADD4-ADD5 and pulls its Y3 output low to clear SYS/LOC latch U27-9. When the CPU executes an I/O write to onboard port A0H, U34 pulls its Y2 output low to set SYS/LOC latch U27. The state of the SYS/LOC latch is applied to one input of Address Map Decoder U30. (Refer to paragraph 4-9.)

4-9. ADDRESS MAP DECODING

In each memory read or write cycle, the CPU (via its status signal S2/) drives the IO/$\overline{M}$ signal low to enable Address Map Decoder U30, (Refer to figure 6-1 sheet 5). When enabled, U30 decodes address bits ADDB-ADD13 and the state of SYS/LOC latch U27-9 to provide the appropriate mapping signal to either the system bus, local bus, or DMA bus. The decoding is performed by U30 to produce the mapping signals as follows:

Address	SYS/LOC	Mapping Signal
00000-007FF	1	SEL MBMEM/
00000-007FF	0	SEL DRAM/
00800-EFFFF	X	SEL MBMEM/
F0000-F7FFF	X	SEL DRAM/
F8000-F9FFF	X	SEL SRAM/
FE000-FFFFF	X	SEL ROM/

When asserted, the SEL MBMEM/ mapping signal enables gate U82-3 (5D4) to generate the MB CYC signal and initiate a system bus memory cycle. The SEL DRAM/ mapping signal enables the 8202A Dynamic RAM Controller (sheet 8), which decodes address bits ADDD-ADDE as follows to initiate either a DRAM memory cycle or to enable a local bus I/O or system bus I/O cycle:

ADDE	ADDD	Cycle
0	1	DRAM Memory (para. 4-20)
1	0	System Bus I/O enable (para. 4-11)
1	1	Local Bus I/O enable (para. 4-18)

To enable a system bus I/O cycle, the 8202A first drives MADD6 high and then pulls RAS1/, WE/ and CAS/ low to set Multibus I/O Enable (MBUSIOEN) latch U36-5. To signal the completion of the command to the CPU, the 8202A then asserts SACK/ (system acknowledge) which, together with timing signal T2/, activates ON BD RDY via gate U43-11 (5B3). Timing signal T2/ is activated by U47 (4A3) from the middle of state T_1 until the end of T_2 in every CPU bus cycle. During a subsequent I/O read or I/O write cycle, the CPU (via its status signal S2/) drives the IO/$\overline{M}$ signal high and gates MBUSIOEN through U26-3 (4A2) and U82-3 (5D4) to generate the MB CYC signal and initiate a system bus I/O cycle. The local bus I/O cycle is similar except that MADD6 is driven low and clears U36-5.

4-10. I/O PORT MAPPING

In order to set up the hardware for program access to local (onboard) I/O ports, a CPU memory write must first be executed to any memory location in the 8k segment F6000H-F7FFF. (See figure 4-4.) After the hardware is set up, the I/O ports are mapped as listed in table 4-1.

4-11. SYSTEM BUS INTERFACE

The 8289 Bus Arbiter (2DH) operates in conjunction with the 8288 Bus Controller (2D6) to interface the processor board to the system bus. As discussed in paragraph 4-9, a system memory cycle or a system I/O cycle is initiated by the MB CYC signal, which enables both the 8288 and 8289.

4-12. SYSTEM BUS ARBITRATION

The falling edge of the system BCLK/ signal provides the timing reference for the 8289. When the MB CYC signal is asserted and status signals S0/, S1/, and S2/ indicate a read or write cycle, the 8289 Bus Arbiter pulls BREQ/ low and drives BPRO/ high. The BREQ/ output from each bus master on the system bus is used where bus priority is resolved by a parallel priority scheme. The BPRO/ output from each bus master on the system bus is used where bus priority is resolved by the serial priority scheme.

The 8289 CBRQ/ pin is an open-collector input/output that may be optionally employed in either a serial or parallel priority resolution scheme to request a controlling higher-priority bus master to surrender the system bus to a lower priority bus master. When CBRQ/ is jumpered to ground (always requesting) and CRQLCK/ is high, the 8089 will surrender the bus after each read or write cycle. The DLL firmware drives CRQLCK/ low via onboard I/O port E6 when locking the bus during the transfer of a block of data

Table 4-1. Onboard I/O Port Mapping

I/O Port Address (Hexadecimal)	Function	Description
00 01	Set TXSRT Clear TXSRT	When set via port 00, TXSRT (Transmit Start) indicates to SerDes board that a data packet is ready for transmission to serial link. TXSRT is set by DLL firmware after data packet is formatted in SRAM and 8237-2 DMA Controller channel 0 is initialized. SerDes board TXC (Transmit Complete) signal clears TXSRT after completion of data packet transfer. Port 01 provides software with means to clear TXSRT.
02 03 04	Set RXAV1 Set RXAV2 Set RXAV3	Receive Available signals RXAV1, RXAV2, and RXAV3 indicate to SerDes board that DMA channel 1, 2, or 3 is ready to receive data packet. DLL firmware sets RXAV1 during initialization and selectively sets RXAV1, RXAV2, and RXAV3, as required, after a DMA receive operation is completed.
05	RESET ERROR	Clears Receive Length Error and CRC Error flip-flops on SerDes board to allow next data packet to be received in diagnostic mode. ERROR may be cleared by DLL firmware or by software.
06	Clear Channel Counter	Clears hardware channel counter, causing DMA channel 1 to receive next data packet. Channel counter may be cleared by DLL firmware or by software.
07	Output Pulse Test Point	Reserved for Intel Test Engineering.
80 90	Set System Interrupt Clear System Interrupt	Allows DLL firmware or software to set and clear system interrupts. System interrupt levels 0-7 are user-selectable with switch S1.
A0 B0	Set SYS/LOC Clear SYS/LOC	Allows 8088 CPU to access lower 2k bytes of system memory or lower 2k bytes of local (onboard) DRAM memory. When set (SYS/LOC = 1), the lower 2k of system memory may be accessed. When clear (SYS/LOC = 0), the lower 2k of DRAM memory may be accessed for interrupt vector access and local data storage and retrieval. (Refer to paragraph 4-8.) SYS/LOC may be set or cleared by DLL firmware or by software.
C0-CE	8237-2 Select/Control	DLL firmware access to the following DMA Controller internal registers: C0: Base and Current Address Registers for Channel 0 C1: Base and Current Word Count Registers for Channel 0 C2: Base and Current Address Registers for Channel 1 C3: Base and Current Word Count Registers for Channel 1 C4: Base and Current Address Registers for Channel 2 C5: Base and Current Word Count Registers for Channel 2 C6: Base and Current Address Registers for Channel 3 C7: Base and Current Word Count Registers for Channel 3 C8: Command and Status Registers C9: Request Register CA: Set/Reset Mask Register CB: Mode Register CC: Clear Byte Pointer flip-flop CD: Temporary Register/Master Clear CE: Illegal CF: Mask Register

Table 4-1. Onboard I/O Port Mapping (Cont'd.)

I/O Port Address (Hexadecimal)	Function	Description
D0-D3	8253 Select/Control	DLL firmware access to the following Programmable Interval Timer (PIT) functions: D0: Timer 0 (alarm clock) D1: Timer 1 (real-time clock) D2: Timer 2 (backoff timer) D3: Control Word Register
E0-E3	8255A Select/Control	DLL firmware access to the following Programmable Peripheral Interface (PPI) functions: E0: Port A (input) E1: Port B (output) E2: Port C (input upper four bits; output lower four bits) E3: Control Word Register
F0-F1	8259A Select/Control	DLL firmware access to the following Programmable Interrupt Controller (PIC) functions: F0: Control Words ICW1, OCW2, and OCW3, and Status Register F1: Control Words ICW2, ICW4, and OCW1, and Mask Register

between system memory and onboard memory. The CPU driven LOCK/ signal, which can also lock the bus, is activated by a "lock" prefix instruction and remains active until the completion of the next instruction. This is useful in CPU handshake operations on the system bus.

4-13. SYSTEM BUS CONTROL

The processor board may only gain control of the system bus after the BPRN/ input to the 8289 has been pulled low. On the next falling edge of BCLK/, the 8289 pulls its BUSY/ and AEN/ outputs low. The BUSY/ output indicates to other bus masters that the system bus is in use and will not surrender the bus until it raises BUSY/. The AEN/ signal enables address bus drivers U52, U88, and U89, and the command outputs of the 8288 Bus Controller. The 8288 decodes buffered status signals S0B/, S1B/, and S2B/, activates ALE to strobe the 20-bit address into the address bus drivers, and drives DT/$\overline{R}$ low or high as required to control the direction (input or output) of data bus driver U91. (The DT/$\overline{R}$ signal is driven low when the status signals denote a read bus cycle.) The 8288 then activates the appropriate read or write command and drives DEN high to U82-11, which generates MBDEN/ to enable the outputs of data bus driver U91. (DEN is driven high during T_3 of each read cycle and during T_2, T_3, and T_4 of each write cycle.)

The addressed memory or I/O device, after placing data on the bus (for a read cycle) or accepting data from the bus (for a write cycle), drives XACK/ low to acknowledge the command. Since MBDEN/ is true, XACK/ is driven through gates U25-6 (5A4) and U26-6 to assert ready signal MB RDY. When MB RDY goes high, the 8088 CPU terminates the command. The 8289 Bus Arbiter releases AEN/ to disable the address bus drivers and the 8288 Bus Controller, which pulls DEN low to disable the data bus driver. The 8289 then surrenders the system bus by releasing BREQ/ and BUSY/ and pulling BPRO/ low.

4-14. SYSTEM BUS TIME OUT

The 8088 CPU expects a Transfer Acknowledge (XACK/) to be returned from the addressed system memory or I/O device in response to each read or write command. If a nonexistent memory or I/O device is addressed and an acknowledge signal (XACK/) is not received, the CPU would ordinarily be hung up in a wait state until reset. Bus Time Out one-shot U65-9 (5A5), which provides a failsafe against a CPU hangup (infinite T_W states), is retriggered by the leading edge of the MBDEN/ signal. (MBDEN/ is generated when the 8288 Bus Controller asserts DEN during *each* system read or write cycle.) If the XACK/ signal is not received, U65-9 times out and the trailing edge of the 10-

millisecond pulse clocks and sets latch U27-6. When U27-6 sets, U26-6 generates MB RDY to the CPU. (Refer to paragraph 4-13.)

4-15. SYSTEM BUS INTERRUPT GENERATION

Switch S1 (3C2) allows user selection of system interrupt levels INT0/ through INT7/. The selected interrupt level is set and cleared by an 8088 CPU write to port 80H and 90H, respectively. For onboard I/O operations, the MBUSIOEN/ signal is false, which enables the local 8288 Bus Controller. The 8288 decodes status signals S0/, S1/, and S2/ and generates an Advanced I/O Write (AIOW/) signal. Decoder U34 (5C5) is enabled when AIOW/ is true and address bits ADD6 and ADD7 are high. When enabled, U34 decodes address bits ADD4 and ADD5 to generate the SET INT/ and CLR INT/ signals. The SET INT/ signal sets Multibus Interrupt (MB INT) latch U69 (3C3). The $\overline{Q}$ output of U69 enables gate U66-11, which drives the system interrupt level selected by switch S1. The Q output of U69 generates status signal MB INT, which is applied as an input bit (PA0) to 8255A port A. (Refer to paragraph 4-26.) The CLR INT/ signal is applied through OR-gate U45-8 to clear latch U69 and terminate the system bus interrupt. The system host processor can also clear latch U69 by means of an I/O write instruction as described in paragraph 4-16.

4-16. SYSTEM HOST I/O DECODE

By means of an I/O write instruction, the system host processor can selectively reset the processor board, clear the system bus interrupt, or interrupt the 8088 CPU. Address decoders U87 (3D6) and U90 (3C6), when enabled by an IOWC/ command, decode the 8-bit or 16-bit address on the system bus. Jumper posts are provided at the input of U87 and the outputs of both U87 and U90. A jumper in position E8-E9 (factory installed) accommodates 8-bit I/O address decoding; this jumper may alternatively be removed and reinstalled in position E9-E10 to accommodate 16-bit I/O address decoding. As described in paragraph 2-10, jumper posts are provided at the outputs of U87 and U90 to allow selection of the system I/O address.

When U87 and U90 recognize the selected I/O address, the output of U94-4 goes high and allows divider U83 to begin counting the Constant Clock (CCLK/) cycles. On the second positive-going edge of CCLK/, U83-3 goes low and applies an enabling input to data gates U86-8, U86-11, and U86-6. If DAT0/ is low, the output of U86-8 triggers one-shot U65-5, which generates a 3-microsecond SEL RESET signal to reset the processor board as described in paragraph 4-2. If DAT1/ is low, the output of U86-11 generates the CMD INT/ signal to interrupt the 8088 CPU via the 8259A Programmable Interrupt Controller. (Refer to paragraph 4-27.) If DAT2/ is low, the output of U86-6 clears Multibus Interrupt (MB INT) latch U69.

On the third positive-going edge of CCLK/, U83-14 goes low and generates acknowledge signal XACK/ onto the system bus. When the host processor terminates the I/O command, the output of U49-4 goes low and clears divider U83.

4-17. LOCAL BUS CIRCUITS

As shown in figure 4-1, the local bus is controlled by 8288 Bus Controller U73. Located on the local bus are the Address Decoder (U30), 16k DRAM memory, 8k ROM memory, 8253 Programmable Interval Timer (PIT), 8255A Programmable Peripheral Interface (PPI), and the 8259A Programmable Interrupt Controller (PIC). The DMA channel control logic which is also on the local bus, is described in paragraph 4-28.

4-18. LOCAL BUS CONTROL

Referring to figure 6-1, the 8288 Bus Controller (4B4) is enabled when its CEN input is driven and held high by gate U26-3 in its inhibited state. Gate U26-3 (4A2) is inhibited when the CPU (via its status signal S2/) drives the IO/M signal low during a memory read or memory write cycle (paragraph 4-6) or when MBUSIOEN latch U36-5 (8A4) is clear. Latch U36-5 is cleared automatically by a processor reset (paragraph 4-2), and may be selectively cleared by a CPU memory write to any location within the 8k block F6000H-F7FFFH. As described in paragraph 4-9, a memory write to location F6000H, for example, causes Address Decoder U30 (5D5) to assert the SEL DRAM/ mapping signal to enable 8202 Dynamic RAM Controller U13 (8C5). The 8202 decodes address bits ADDD-ADDE (both logic 1's for onboard I/O), pulls MADD6 low, and then clocks the MBUSIOEN latch to the clear state by pulling RAS1/, WE/, and CAS/ low. As discussed in paragraph 4-6, the 8288 decodes the CPU status signals S0/, S1/, and S2/ to identify the CPU cycle and generate the appropriate command and control signals for local bus control.

When enabled, the 8288 generates the ALE signal during state T_1 of each CPU bus cycle. (See figures 4-1, 4-2, and 4-3.) The trailing edge of ALE strobes the 20-bit address into address latches U53, U55, and U71. The ALE signal also strobes the lower 16 bits of

the 20-bit address into address latches U56 and U72 when the CPU has control of the DMA bus. (Refer to paragraph 4-30 through 4-32.)

4-19. ADDRESS DECODE

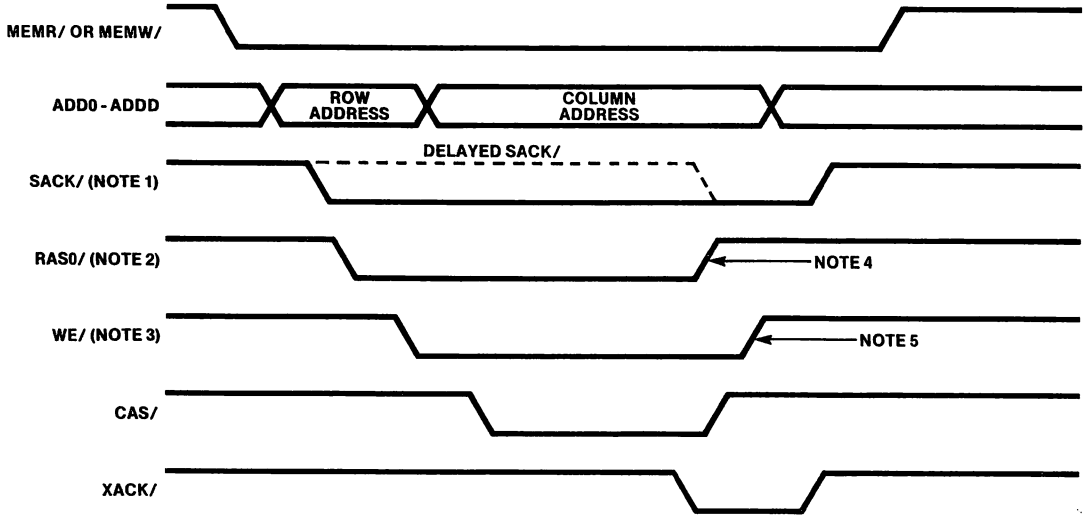
A local bus cycle is initiated when the Local Cycle (LOC CYC) signal is generated by gate U44-13 (5D3). The LOC CYC signal is combined with the 8288 Data Enable (DEN) signal to enable local bus data buffer U32 (4D3). Gate U44-13 is enabled when the MB CYC and SEL SRAM/ signals are false (paragraph 4-9) and I/O decoder U34 (5B5) asserts either the SEL 53/, SEL 55/, or SEL 59/ select signal. Stated in other terms, LOC CYC is true when the 8088 CPU writes to the 16k DRAM memory, 8k ROM memory, 8253 PIT, 8255A PPI, or the 8259A PIC.

Timing signal T2/ is active low from the middle of state T_1 until the end of state T_2 in every machine cycle. When T2/ goes high at the beginning of state T_3, the LOC CYCLE signal generates ON BD RDY via gate U43-11 (5B3) to acknowledge receipt of CPU read or write command to the 8253, 8255A, or 8259A, or a CPU read command to ROM memory. The 8202A Dynamic RAM Controller generates its own acknowledge as described in paragraph 4-21.

4-20. DRAM MEMORY

The onboard 16k physical address block F0000-F3FFF is allocated to DRAM memory. (See figure 4-4.) As discussed in paragraph 4-9, Address Map Decoder U30 (5D5) decodes the CPU memory address to generate the appropriate mapping signal. The 8202A Dynamic RAM Controller (8C5) is enabled when U30 drives the SEL DRAM/ signal low. Because its REFRQ input is tied low, the 8202A operates in the automatic refresh mode and will delay a read or write request if a refresh cycle is in process.

4-21. READ ACCESS CYCLE. When the 8202A is enabled, a read access cycle is initiated when the 8288 Bus Controller (4B4) asserts the MEMR/ signal. (Refer to figure 4-5.) The 8202A begins the cycle by multiplexing address bits ADD0-ADD6 onto its output lines, activating the System Acknowledge (SACK/) signal to indicate the beginning of the cycle,



NOTES:
1. SACK/ IS DELAYED IF REFRESH IS IN PROGRESS.
2. RAS0/ IS ASSERTED IF ADDE = 0.
3. WE/ IS PULLED LOW ONLY DURING WRITE CYCLE.
4. READ DATA VALID ON RAM DATA OUTLINES.
5. RAM LATCHES WRITE DATA.

Figure 4-5. DRAM Memory Access Cycle Timing 121746-14

and pulling the Row Address Strobe (RAS0/ or RAS1/) low depending on the state of address bit ADDE. When ADDE=0, RAS0/ is pulled low to strobe the row address into the 16k RAM chips. The 8202A then multiplexes address bits ADD7-ADDD onto its output lines, activates the Transfer Acknowledge (XACK/) signal, and pulls the Column Address Strobe (CAS/) low to strobe the column address into the RAM chips. When RAS0/ is subsequently released, the RAM chips output the valid data byte onto the D0-D7 lines. The trailing (positive-going) edge of XACK/ clocks the data on the RAM chip data output lines into latch U33 (8A5), which transfers the data byte onto the DATA0-DATA7 bus. (The output of U33 is enabled when SEL DRAM/ and MEMR/ are asserted.)

If a refresh cycle is in progress, the SACK/ signal is delayed until the beginning of XACK/. SACK/ generates the RAM AACK/ acknowledge signal which, when timing signal T2/ goes high, activates ON BD RDY via gate U43-11 (5B3).

4-22. WRITE ACCESS TIMING. A write access cycle is similar to a read access cycle except that the 8288 Bus Controller asserts MEMW/ and pulls Write Enable (WE/) low before CAS/. Data bits DATA0-DATA7 are latched into RAM on the trailing (positive-going) edge of WE/. The output of latch U33 is disabled during the cycle because MEMR/ is inactive.

4-23. ROM MEMORY

The onboard 8k physical address block FE000-FFFFF is allocated to ROM memory. (See figure 4-4.) This memory is contained in two 2732A EPROM chips, each of which contains 4k bytes. Chip U59 (6D6) contains the lower 4k bytes and U58 (6C6) contains the upper 4k bytes. When the CPU executes a memory write to this physical address block, Address Map Decoder U30 asserts the SEL ROM/ signal to one of the two enabling inputs of gates U35-11 and U35-3. The second enabling input to these two gates is address bit ADDC. If ADDC=0, the output at U35-3 goes low and enables U59; if ADDC=1, the output at U35-11 goes low and enables U58. The enabled 2732A decodes address bits ADD0-ADDB and, when the 8288 Bus Controller asserts MEMR/, places the contents of the addressed location on the DATA0-DATA7 lines. The acknowledge signal is generated as described in paragraph 4-19.

4-24. LOCAL I/O DECODE

Decoder U34 (5B5) is enabled via gate U3-8 when the CPU excutes an I/O write to any location with the C0H-FFH address range. Once enabled, U34 decodes address bits ADD4-ADD5 as follows to generate the appropriate select signal:

ADD5	ADD4	Select Signal
0	0	SEL 37/
0	1	SEL 53/
1	0	SEL 55/
1	1	SEL 59/

4-25. PROGRAMMABLE INTERVAL TIMER

The 8253 PIT (7D5) is enabled when U34 asserts the SEL 53/ select signal. When U34 asserts SEL 53/, the 8253 PIT examines IOR/, AIOW/, and address bits ADD0-ADD1 to execute the following:

IOR/	AIOW/	ADD1	ADD0	Operation
1	0	0	0	Load Timer 0
0	1	0	0	Read Timer 0
1	0	0	1	Load Timer 1
0	1	0	1	Read Timer 1
1	0	1	0	Load Timer 2
0	1	1	0	Read Timer 2
1	0	1	1	Write Mode Word
0	1	1	1	No Operation

The DLL firmware initializes Timers 0 and 1 to operate in mode 0 (interrupt on terminal count) and Timer 2 to operate in mode 2 (divide-by-N counter). As listed in table 4-1, Timers 0, 1, and 2 function as the controller alarm clock, real-time clock, and backoff timer, respectively.

Flip-flop U69 (7A5) divides the 2.5-MHz PCLK clock by two to develop the 1.25-MHz clock for all three timers, allowing a count resolution from 0.8 microsecond to 52.4 milliseconds. On reaching terminal count, Timers 0, 1, and 2 generate interrupt levels IR5, IR6, and IR7, respectively, to the 8259A PIC. (Refer to paragraph 4-27.) Stopping and starting of all three timers is controlled by DLL firmware or software.

4-26. PROGRAMMABLE PERIPHERAL INTERFACE

The 8255A PPI (6B5) is enabled when U34 asserts the SEL 55/ select signal.

The DLL firmware initializes the 8255A to operate in mode 0; in this mode, Port A and the upper half of Port C are input ports and Port B and the lower half

of Port C are output ports. When U34 asserts SEL 55/, the 8255A PPI examines IOR/, AIOW/, and address bits ADD0-ADD1 to execute the following:

IOR/	AIOW/	ADD1	ADD0	Operation
1	0	0	0	Write Port A
0	1	0	0	Read Port A
1	0	0	1	Write Port B
0	1	0	1	Read Port B
1	0	1	0	Write Port C
0	1	1	0	Read Port C
1	0	1	1	Write Control Word
0	1	1	1	No Operation

Bit assignments for Port A, Port B, and Port C are listed and described in table 4-2.

4-27. PROGRAMMABLE INTERRUPT CONTROLLER

The 8259A PIC (7D5) is enabled when U34 asserts the SEL 59/ select signal. When U34 asserts SEL 59/, the 8259A examines IOR/, AIOW/, and address bit ADD0 to execute the following:

IOR/	AIOW/	AD0	Operation
1	0	0	Load ICW1, OCW2, OCW3
1	0	1	Load ICW2, ICW4, OCW1
0	1	0	Read Status Register
0	1	1	Read Mask Register

The DLL firmware initializes the 8259A PIC to operate as follows:

a. Sets edge-triggered mode; i.e., interrupt request sensed on positive-going edge of IR0-IR7.

b. Programs the five most-significant bits of vector byte (8289A automatically supplies the three least-significant bits).

c. Sets automatic end-of-interrupt mode; i.e., automatically clears internal in-service bit during second INTA cycle.

After initialization, the 8259A will detect an edge-triggered (positive-going) interrupt request from the following sources:

IR0—DMA Channel 1 (receive complete)

IR1—DMA Channel 2 (receive complete)

IR2—DMA Channel 3 (receive complete)

IR3—DMA Channel 0 (transmit complete)

IR4—Wakeup (host processor has data)

IR5—Timer 0 (alarm clock timeout)

IR6—Timer 1 (real-time clock timeout)

IR7—Timer 2 (backoff timer timeout)

When the 8259A senses an interrupt request, it interrupts the 8088 CPU by driving INT high. Assuming that the CPU interrupts are not masked nor disabled, the CPU completes the current instruction and executes the first of two back-to-back interrupt acknowledge cycles. During the first interrupt acknowledge cycle, the CPU drives status signals S0/, S1/, and S2/ low. The 8288 Bus Controller, which is enabled whenever the MBUSIOEN latch is clear, decodes the status signals and asserts INTA/ and ALE. When ALE goes high, the status signals enable gate U3-6, which drives INT CYC/ low and disables I/O Decoder U34. When the first INTA/ goes low, the 8259A freezes the state of its internal priority resolution logic. At the end of state T_2, timing signal T2/goes high and, via gate U26-6, drives MB RDY high to acknowledge the first INTA/ signal. The CPU then executes the second interrupt acknowledge cycle, which is similar to the first except for the action of the 8259A. When the second INTA/ goes low, the 8259A places an 8-bit identifier on the data bus. The 8088 CPU inputs the 8-bit identifier, terminates the interrupt acknowledge cycle, and multiplies the 8-bit identifier by four to derive the appropriate vector address.

4-28. DMA BUS

As shown in figure 3-2, the 8237-2 DMA Controller, 8k SRAM memory, discrete DMA Bus Arbiter, and associated drivers and latches are located on the DMA bus. The DMA I/O Latch and DMA Receive Channel Sequencer are located on the local bus.

The 8237 operates in either the inactive or active cycle, and can assume one of seven states, each of which is composed of one clock period. (See figure 4-6.) State S_I is the inactive state, which is entered when the 8237 has no valid DMA requests pending. While in state S_I, the 8237 is inactive but may be programmed by the 8088 CPU. States S_0 through S_4 comprise the active cycle. State S_0 is the first state of a DMA service during which the 8237 initiates a Hold Request (HREQ) but the Discrete DMA Bus Arbiter has not returned Hold Acknowledge (HLDA). When HLDA is asserted, the 8237 proceeds into working states S_1, S_2, S_3, and S_4 and processes the DMA request.

When no channel is requesting service, the 8237 enters the S_I state and samples Data Request lines TXRQ, DREQ1, DREQ2, and DREQ3 every clock cycle to ascertain if any channel is requesting service. During the S_I state, the 8237 also samples the SEL 37/ line every clock cycle to ascertain if the 8088

Table 4-2. 8255A PPI Bit Assignments

Bit	Mnemonic	Signal Definition
		PORT A (INPUT)
PA0	MBINT	Multibus Interrupt: 1 = processor board currently interrupting host processor.
PA1	HLDA	Hold Acknowledge: 1 = 8237-2 DMA Controller currently controlling DMA bus.
PA2	CS	Carrier Sense: 1 = carrier detected on coaxial cable.
PA3	ENABLE TXD	Enable Transmit Data: 1 = packet transmission in process.
PA4	LEN ERR	Length Error: 1 = last packet received longer than maximum allowable size.
PA5	CRC ERR	Cyclic Redundancy Check Error: 1 = last packet received contained CRC error.
PA6	TXTO	Transmission Time Out: 1 = last packet transmission exceeded 3.5 milliseconds.
PA7	TX CLSN	Transmission Collision: 1 = last packet transmission encountered collision.
		PORT B (OUTPUT)
PB0	CLR SER	Clear SerDes Board: 1 = initialize SerDes board hardware. Both PB6 (RXEN/) and PB7 (TXEN/) should be false (high) before asserting CLR SER.
PB1	READ ADD/	Read Address: 0 = read node address stored in SerDes board ROM. Immediately causes pseudo-DMA receive transfer. PB6 (RXEN/) should be false (high) before asserting READ ADD/.
PB2	FRC CRC	Force CRC Error: 1 = transmit packet with bad CRC.
PB3	PROMISCUOUS RCV/	Promiscuous Receive: 0 = receive (interrupt) all packets regardless of packet address.
PB4	NORMAL MODE	Normal/Diagnostic Mode: 1 = normal mode, 0 = diagnostic mode. The value of PB4 determines what is done on a receive error. In normal mode, receive CRC error causes automatic initialization of DMA channel being used and Receive Complete (RXC) interrupt will not be generated. In diagnostic mode, no automatic initialization will occur but RXC interrupt will be generated and allow DMA channel to be read.
PB5	VERIFY ON BRD/	Verify On Board: 0 = SerDes loopback. SerDes board simultaneously transmits and receives same data packet; packet does not go out over transceiver cable and does not get written back into SRAM memory. CRC generation and checking on same packet act as transmit and receive verification.
PB6	RXEN/	Receive Enable: 0 = true. Enables SerDes board receive logic. RXEN/ is normally true.
PB7	TXEN/	Transmit Enable: 0 = true. Gates transmit data packet to transceiver.
		PORT C (OUTPUT)
PC0	VERIFY XCVR/	Verify Transceiver: 0 = transceiver loopback. Similar to VERIFY ON BRD/ (PB5) except tests transceiver cable as well.
PC1	none	Used in power-up confidence test diagnostic: 1 = LED on (test failed); 0 = LED off (test passed).
PC2	CRQ LCK/	Common Request Lock: 0 = true. Prevents 8289 Bus Arbiter from surrending bus to lower priority device during block transfer of data over system bus.
PC3	none	Not used.
		PORT C (INPUT)
PC4 PC5 PC6	none none none	For system compatibility, allows user to choose starting address in one of eight jumper-selectable command blocks. (Refer to paragraph 2-13.)
PC7	none	Test purposes only. With plug-in jumper installed, firmware confidence test will loop repeatedly on power-up or reset. (Refer to table 2-6).

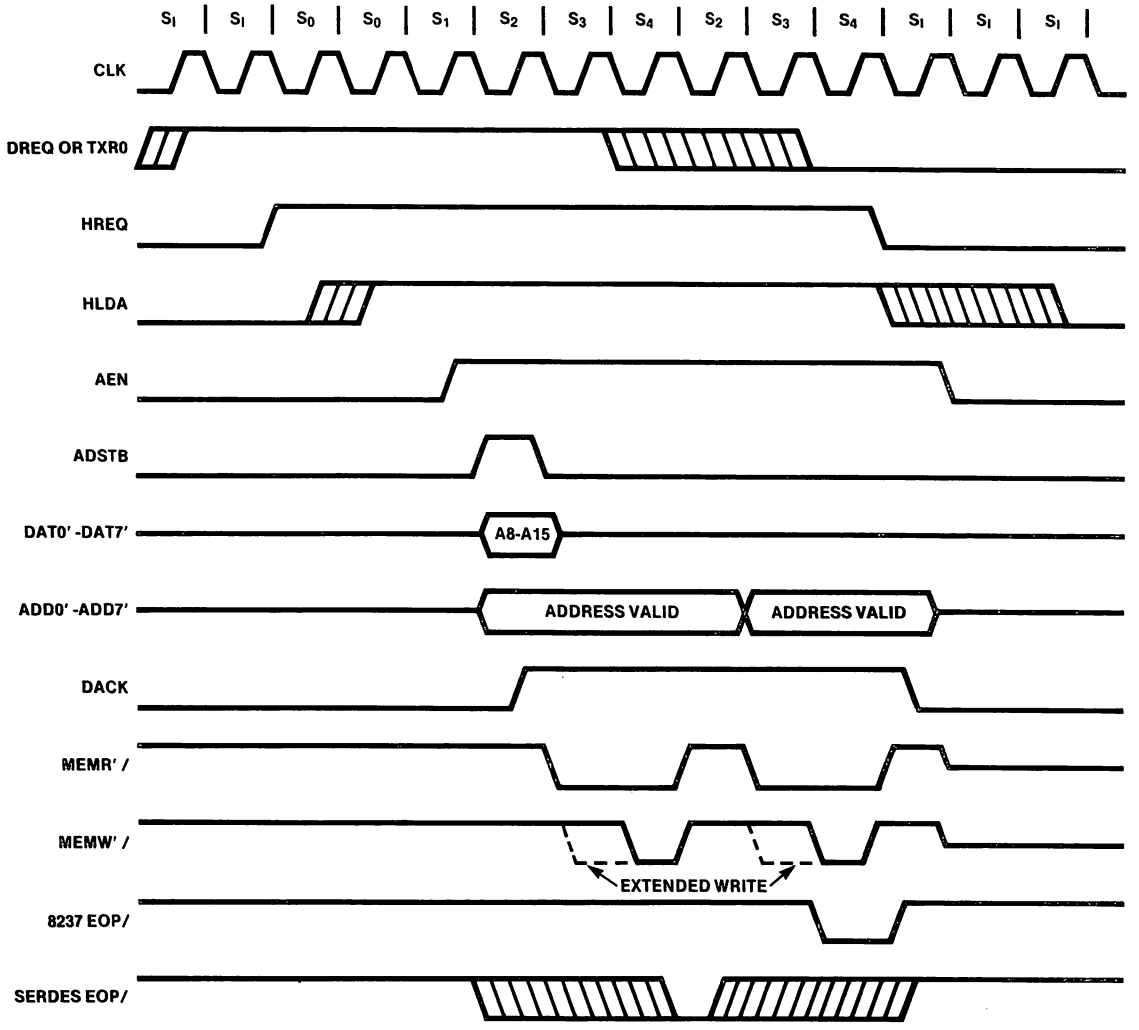


Figure 4-6. DMA Transfer Timing 121746-15

CPU is attempting to read or write to the 8237 internal registers. When SEL 37/ is asserted and HREQ is inactive, the 8237 enters its program condition during which the 8088 CPU can read from or write to the internal register, as selected by the contents on address lines ADD0'-ADD3'. (When the 8237 is in its inactive state, the bidirectional IOR'/ and IOW'/ lines select and time the 8088 CPU read and write operations.)

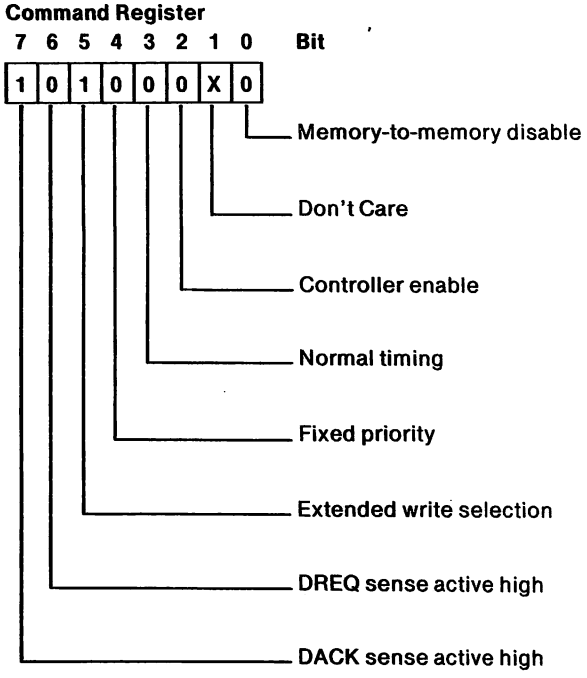
The DLL firmware programs the block transfer mode for the transmit channel (channel 0). In the block transfer mode, the 8237 will continue making DMA transfers (writes) until its Current Word Count register decrements to zero. (TXRQ need not be held active during the entire block transfer.)

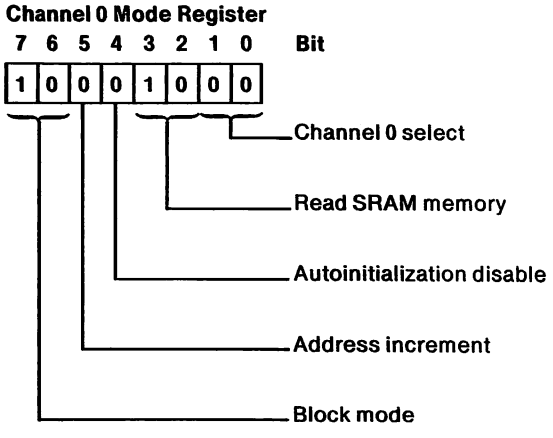
For all three receive channels (channels 1, 2, and 3), the DLL firmware programs the demand transfer mode. In this mode, the 8237 will continue making DMA transfers (reads) until either the Current Word Count register decrements to zero, the SerDes board asserts the EOP/ signal, or the SerDes board deactivates the DREQ signal by generating a Receive Complete (RXCMP) pulse. The EOP/ signal (when asserted) causes the 8237 to autoinitialize, which

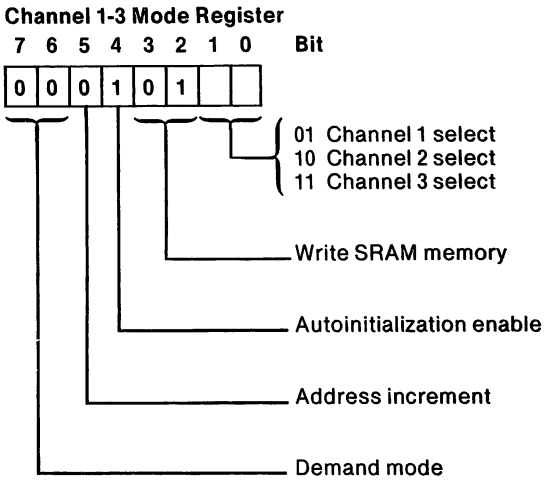
restores the original values in the Current Address and Current Word Count registers of the last service channel. Following autoinitialization, the channel is ready to perform a receive operation without 8088 CPU intervention.

4-29. 8237 INITIALIZATION

When the 8088 CPU executes an I/O read or write to location C0H-CEH, Decoder U34 (5D5) generates the SEL 37/ signal to enable the 8237 to enter its program condition. The 8088 CPU, under control of the DLL firmware, initializes the 8237 Command and Mode registers as follows:





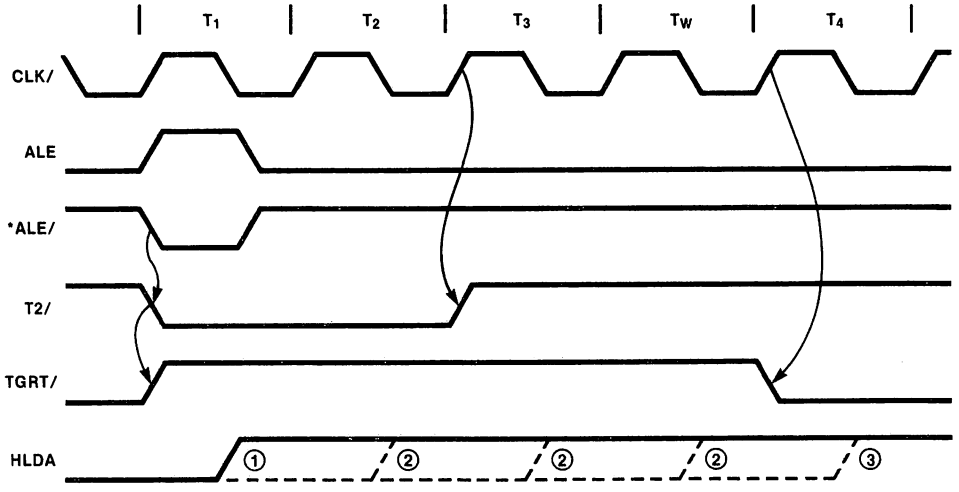


There are no hardware restrictions on the use of any of the 8237 internal registers except the Command and Mode registers. After the Command and Mode registers are thus initialized, the DLL firmware loads the 8237 Base Address register for each DMA channel with an initial value. (In the 8237 address space, location 0000H corresponds to the first location in SRAM memory; i.e., location F0000H in the 8088 CPU address space.) After DMA operation has begun, the Base Address register for each channel is dynamically reloaded to accommodate the available SRAM memory resources.

The DLL firmware also loads a count of 1521 into the 8237 Base Word Count register of the three DMA receive channels. The count of 1521 represents the maximum frame size plus 3 bytes for the SerDes board receive startup and shutdown.

4-30. DMA BUS ARBITRATION

When any one of the four data requests (TXRQ, DREQ1, DREQ2, and DREQ3) is asserted, the 8237 activates HREQ. When HREQ goes high, the discrete Bus Arbiter locks out 8088 CPU access to the DMA bus address, data, and command lines as shown in figure 4-7. (The discrete bus arbitration logic is shown at the top of figure 6-1, sheet 10.) For example, if the 8088 CPU is in state T_1 (ALE/ active) when HREQ goes high, flip-flop U46 is set on the following negative-going edge of CLK/. When set, U46-7 simultaneously disables data buffer U57 and presets (sets) latch U67; U46-9 disables address latches U56 and U72; and U67-9 disables command buffer U74. With U69-9 high, flip-flop U51 sets on the following positive-going edge of CLKB and asserts Hold Acknowledge (HLDA) and its complement HLDA/. The HLDA signal is used as a status bit to Port A of the 8255A PPI (see table 4-2) and to the 8237 as an indication that the 8237 has control of



FOLLOWING HREQ, HLDA IS GENERATED ON THE FIRST FALLING EDGE OF CLK/ WHEN ONE OF THE FOLLOWING CONDITIONS ARE TRUE:

1. 8088 CPU IS IN STATE T_1. CPU ACCESS TO DMA BUS ADDRESS, COMMAND, AND DATA LINES ARE TURNED OFF BEFORE CPU ASSERTS COMMAND.
2. 8088 CPU IS IN STATE T_2, T_3, or T_W AND CPU IS NOT USING DMA BUS; I.E., DMAB CYC/ SIGNAL IS FALSE.
3. 8088 CPU IS IN STATE T_4 (FOLLOWING ONE OR MORE T_W STATES) OR IN T_I (IDLE) STATE. THIS PERMITS 8237 ACCESS TO DMA BUS WHEN CPU CYCLES ARE NOT BACK-TO-BACK.

Figure 4-7. DMA Bus Grant Timing 121746-16

the DMA bus. The HLDA signal is also supplied to the SerDes board to condition its Data Ready (DRDY) handshake logic. The HLDA/ signal, via U43-11 (5B2), generates ON BD RDY to Clock Generator U70.

4-31. DATA RECEPTION

The outputs of I/O latch U17 are used to selectively clear the DMA Receive Channel Sequencer, to signal the SerDes board that a receive channel is available, or to inform the SerDes board that a data packet is ready for transmission. The DLL firmware initially executes an I/O write to location 07H and then to location 02H. The write to location 07H clears the DMA Receive Channel Sequencer, which is composed of quad D-type flip-flop U37 (9B6) and gates U19 and U60. The write to location 02H sets RXAV1 high to generate Receive Available (RXAV/) to the SerDes board. The three DMA receive channels operate in a rotating mode so that back-to-back data packets from the serial link may be received at the maximum throughput rate. The receive channels are rotated by the sequencer after each data packet is stored in SRAM memory. During the following discussions of the DMA bus logic involved in receiving a data packet, assume that RXAV1 is set and U37 is clear; i.e., 1Q, 2Q, and 3Q are low.

The SerDes board, when ready to input a data packet to the processor board, places the first byte on the SDI0-SDI7 lines, outputs a Transfer (XFER) pulse to latch the data into buffer U94 (11D3), and asserts Data Ready (DRDY). The SerDes board then pulls Receive Request Synchronized (RXRQS/) low to generate DREQ1 via gate U60-4. When DREQ1 goes high, the 8237 asserts HREQ to begin DMA bus arbitration. After HLDA goes high, indicating that the 8237 has control of the DMA bus, the 8237 drives both AEN and ADSTB high and outputs the 16-bit address as determined by its Current Address register. (Address bits A8-A15 are multiplexed onto the DAT0′-DAT7′ lines.) When the 8237 pulls ADSTB low, U77 latches A8-A15 and transfers A8-A12 onto address lines ADD8′-ADDC′. (Notice that the most-significant address bits are not used.) The 8237, after asserting I/O Read (IOR′/) to enable read buffer U94 to transfer the data byte onto the DATA0′-DATA7′ lines, pulls MEMW′/ low.

Decoder U97 (10A4), which is enabled on the negative-going edge of MEMW'/, decodes ADDA'-ADDC' to select one of the eight 1k byte banks of SRAM memory. When the 8237 releases MEMW'/, the data byte is latched into SRAM memory. MEMRW/ is generated by MEMW'/ or MEMR'/. When MEMRW/ goes high, the SerDes board terminates DRDY. This sequence is repeated while incrementing the 8237 Current Address register and decrementing the Current Word Count register, until the last data byte has been transferred.

As shown in figure 4-6, the 8237 executes state S_I only when the updating of the most-significant address bits is necessary. Thus, on a long data transfer, state S_I occurs only once in 256 transfers. When the last incoming data byte has been transferred, the SerDes board generates the Receive Complete (RXCMP) pulse. The leading edge of RXCMP, via gate U19-8 (9B5), drives the Receive Complete (RXC1/) signal low. The trailing edge of RXCMP clocks (rotates) flip-flop U37, which deactivates DREQ1 and sets up the logic to activate DREQ2 when the SerDes board again asserts RXRQS/. The trailing edge of RXCMP allows RXC1/ to go high and generate an interrupt request via the 8259A PIC.

Part of the interrupt service routine for each of the three receive channels is to inform the SerDes board that a receive channel is available. This action is performed by the CPU executing an I/O write to location 02H, 03H, or 04H, respectively, to generate RXAV1, RXAV2, or RXAV3. Either of these signals, when asserted, generates RXAV/ to the SerDes board.

When DREQ1 goes low, the 8237 pulls AEN low to initiate the release of the DMA bus as shown in figure 4-8. The AEN signal, rather than HREQ, initiates the release of the DMA bus because the 8237 may still be driving the bus for one clock cycle after HREQ is released.

As mentioned previously, the receive channel's Base Word Count register is initialized with a count of 1521, which is three counts greater than the maximum valid frame size. If the Current Word Count register decrements to zero, the 8237 autoinitializes and asserts the End of Process (EOP/) signal to the SerDes boards to indicate that the frame exceeds the maximum allowable size. In this case the SerDes board drives the LEN ERR status bit true and pulls DREQ1 low to release the DMA bus.

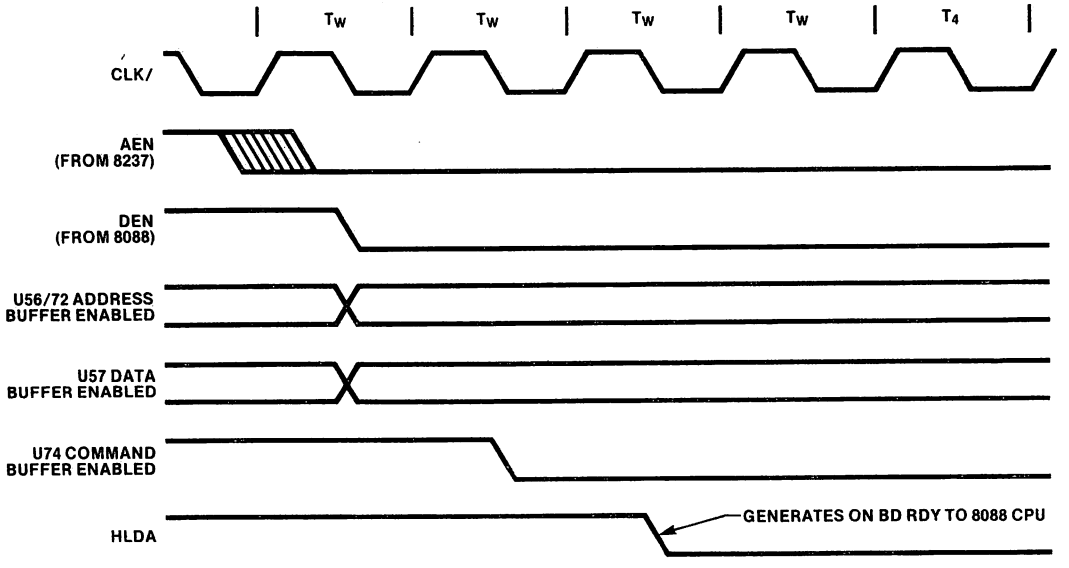


Figure 4-8. DMA Bus Release Timing 121746-17

4-32. DATA TRANSMISSION

After the 8088 CPU stores a formatted data packet in SRAM memory and initializes the DMA transmit channel (channel 0) with the word count and base address, the 8088 CPU executes an I/O write to location 00H to generate the Transmit Start (TXSRT) command. After TXSRT goes high, the SerDes board outputs Transmit Request (TXRQ) to the 8237. When TXRQ goes high, the 8237 asserts HREQ to begin DMA bus arbitration as described in paragraph 4-31.

Upon receipt of HLDA from the DMA Bus Arbiter, the 8237 drives both AEN and ADSTB high and outputs the 16-bit address of the first data byte stored in SRAM memory. (See figure 4-6.) The 8237, after asserting I/O Write (IOW) to enable write buffer U95 (11C3), pulls MEMR'/ low. Decoder U91 (10A4), which is enabled on the negative-going edge of MEMR'/, decodes ADDA'-ADDC' to select one of the eight 1k byte banks of SRAM memory. When enabled, the selected bank outputs the data from the location pointed to by address bits ADD0'-ADD9'. This data byte is transferred through write buffer U95 to the SerDes board. When the 8237 subsequently releases MEMR'/, generating MEMRW/, the SerDes board releases DRDY, processes the data byte, and outputs DRDY to request the next byte. The 8237 then increments its Current Address register and decrements its Current Word Count register. This transfer process is repeated until the Current Word Count register is decremented to zero, upon which the 8237 asserts End of Process (EOP/) and autoinitializes its Current Address register and Current Word Count register; i.e., restores the original contents into the Current Address register and Current Word Count register.

When the SerDes board pulls TXRQ low in response to EOP/, the 8237 pulls AEN low to initiate the release of the DMA bus as shown in figure 4-8. After the SerDes has completed the data packet transfer, it pulls Transmit Complete (TXC/) low to generate an interrupt request via the 8259A and to clear TXSRT.

CHAPTER 5
SERDES BOARD
THEORY OF OPERATION

5-1. INTRODUCTION

The SerDes board schematic diagram is provided in figure 6-2 (8 sheets). Signals that traverse from one sheet to another are identified by a small square at the end of the signal line followed by the sheet number of the signal source or destination (e.g., —□ 8). Both TTL and ECL logic are employed on the SerDes board. The Manchester Encoder, Manchester Decoder, and the transceiver-interfacing differential line drivers and receivers use ECL logic; the remainder of the board is of TTL design.

In the TTL logic, both active-high and active-low signals are used. A signal mnemonic that ends with a slash (e.g., TXRQ/) denotes that the signal is active low (≤0.4V). Conversely, a signal mnemonic without the slash (e.g., TXRQ) denotes that the signal is active high (≥2.0V). Inputs and outputs of the ECL differential line drivers and receivers are ±700 millivolts nominal.

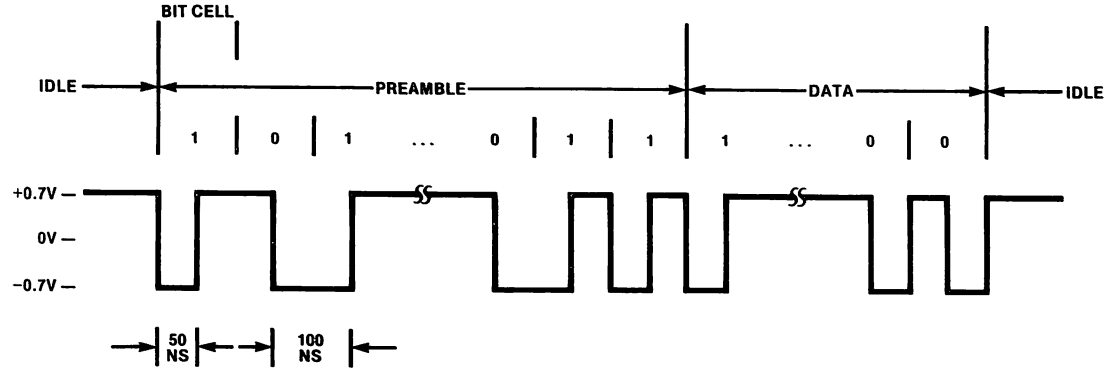
Described in the following paragraphs are the logic and timing involved in transmit, receive, read address, verify SerDes, and verify transceiver sequences. Alphanumerics in parentheses noted in the following paragraphs are provided to assist in the location of specific logic components on the schematic diagram. For example, alphanumerics (4D6) locate a component on sheet 4 in zone D6.

5-2. TRANSCEIVER CABLE WAVEFORM

A typical transceiver cable waveform is illustrated in figure 5-1. The carrier, which is detected as transitions in the middle of the 100-nanosecond bit cells, repetitively triggers a 300-nanosecond one-shot; the carrier is considered lost, indicating the end of a data packet, when the one-shot times out. As shown in figure 5-1, the idle state of the transceiver is +700 millivolts; the transition in the middle of the first bit cell must be positive-going (logic 1), and the transition in the middle of the last bit cell must be negative-going (logic 0).

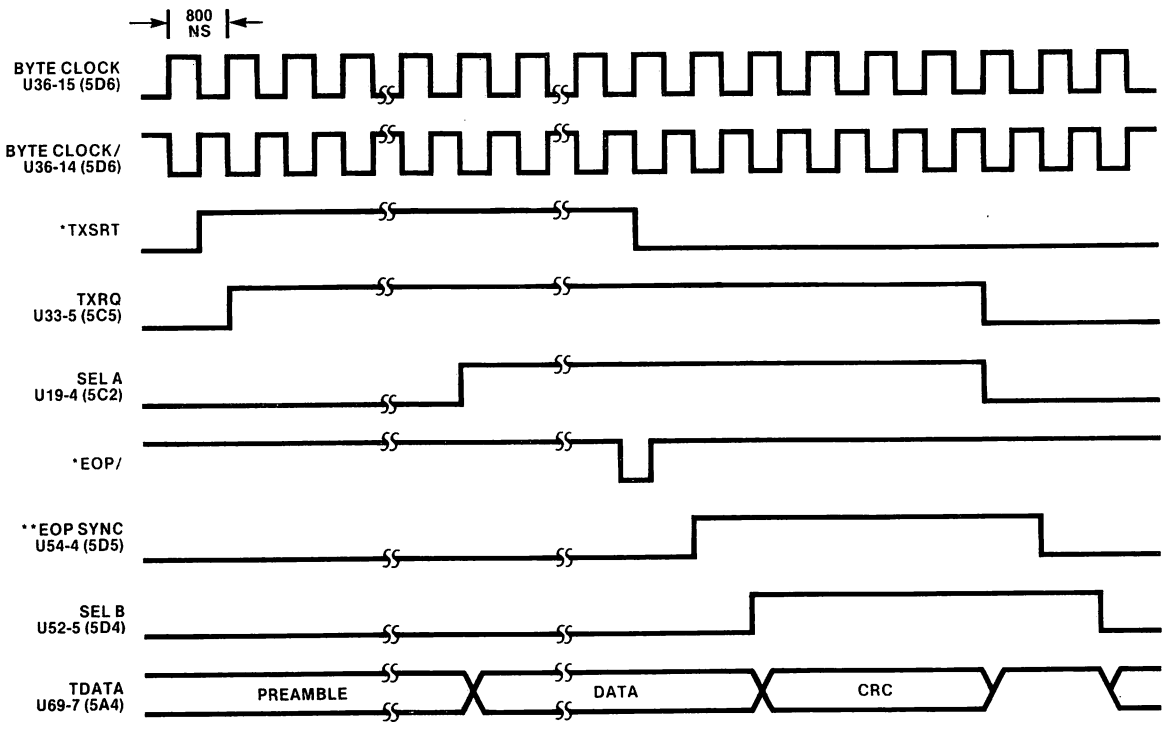
5-3. TRANSMIT SEQUENCE

The transmit framing logic is shown on sheet 5 of figure 6-2, and the associated timing diagram is presented in figure 5-2. The 10-MHz SerDes Clock (SCLK) provides the basic timing reference to the 800-nanosecond byte clock U36 (5D8). Notice that the byte clock provides two complementary outputs referred to in the following discussion as BYTE CLOCK (U36-15) and BYTE CLOCK/ (U36-14).



NOTES:
1. VOLTAGES MEASURED DIFFERENTIALLY AT OUTPUT OF TRANSCEIVER CABLE DRIVER.
2. RISE AND FALL TIMES MEET 10,000 SERIES ECL REQUIREMENTS

Figure 5-1. Typical Transceiver Cable Waveform 121746-18



*SIGNAL FROM PROCESSOR BOARD.
**FOR DESCRIPTION PURPOSES ONLY. EOP SYNC NOT SHOWN ON SCHEMATIC.

Figure 5-2. Transmit Framing Timing 121746-19

5-4. TRANSMIT START UP

After the formatted data packet has been assembled in SRAM memory and the DMA transmit channel initialized, the processor board asserts Transmit Start (TXSRT) to the input of AND-gate U34 (5B6). Timer U16 (5C7), which ensures that the minimum inter-packet gap requirement is met, monitors the Carrier Sense (CS/) line and is repetitively cleared as long as CS/ is active low. When CS/ goes high, U16 begins to count the 3.2-microsecond clock pulses generated by flip-flop U35-8. After the third clock pulse, U16-6 goes high and enables U34-11. On the rising edge of the next BYTE CLOCK/ pulse, flip-flop U33 sets and generates Transmit Request (TXRQ), which (1) enables Preamble Generator U70 (5A5), (2) enables Preamble Byte Counter U51 (5C5), and (3) generates Enable Transmit Data (ENABLE TXD) via flip-flop U91-9. The ENABLE TXD signal (1) enables the ECL transmitter and (2) transmits a status bit to the processor.

5-5. TRANSMIT FRAMING

Data Selector U69 (5A4) multiplexes the preamble, data, and frame check sequence (FCS) inputs onto the Transmit Data (TDATA) line as determined by the following inputs to its A and B select lines:

Select Line		Input
B	A	
0	0	1C0: Preamble
0	1	1C1: Data
1	0	1C2: Ground (Shutdown)
1	1	1C3: FCS

When its preset input goes high, Preamble Generator U70-5 begins generating a series of alternate ones and zeros at a 100-nanosecond rate as determined by the 10-MHz bit clock signal. Seven bytes after TXRQ goes true, Preamble Byte Counter U51-16 sets and applies a high input to AND-gate U68 (5C6) and the

set side of flip-flop U92 (5C2). On the following rising edge of BYTE CLOCK, the output of AND-gate U68 goes high and (1) presets the Preamble Generator via OR-gate U71-6, (2) sets Parallel/Serial Converter U89 (5B7) to the parallel-in mode, and (3) supplies the Transmit Transfer (TXFER/) signal to the Data Ready (DRDY) handshake logic. Preamble Generator U70, after generating the first seven bytes of the 64-bit preamble and just prior to being preset, generates an additional six bits of alternate ones and zeros. Immediately upon being preset, U70 generates two consecutive ones to indicate the end of the preamble and the start of data.

While the preamble is being generated, the DMA controller on the processor board has gained control of the DMA bus and placed the first data byte on the SDO0-SDO7 lines. After the preamble is generated, the rising edge of the next BYTE CLOCK/ sets flip-flop U92 (5C2), which (1) releases Transmit CRC Preset (TXCRC PR/) and (2) enables AND-gate U19. The TXCRC PR/ signal, which is now false, is multiplexed through Data Selector U62 (7A5) to enable the CRC feedback register and allow it to operate on the ensuing serial data stream appearing on the TXCRC DATA line. The output of U19-4 applies a high input to the A select line, causing U69 to multiplex the ensuing serial data stream from Parallel/Serial Converter U89 onto the TDATA line. The falling edge of BYTE CLOCK inhibits AND-gate U68-6, which (1) sets Parallel/Serial Converter U89 to the serial-out mode and (2) generates Transfer (TXFER) to the Data Ready (DRDY) handshake logic. Upon being set to the serial-out mode, U89 shifts out the eight bits of the first byte at a 100-nanosecond per bit rate as determined by the 10-MHz SerDes Clock (SCLK). The first and subsequent bytes are shifted onto the TXCRC and TDATA lines while BYTE CLOCK is active high. While BYTE CLOCK is low, the next byte to be transferred is loaded into U89 from the SDO0-SDO7 lines.

Synchronization of byte transfers between the processor board and the SerDes board is accomplished by the Data Ready (DRDY) handshake logic, which is composed of flip-flops U67-5 (6A6), U84-9, U84-5, and associated gates. When TXFER/ is asserted by the SerDes board, U67-5 sets and, in turn, presets U84-9. On the rising edge of Data Ready Clock (DRCLK) from the processor board, U84-5 sets and asserts DRDY to the processor board. After DRDY goes true, the processor board places the first (next) data byte on the SDO0-SDO7 lines and releases Memory Read Write (MEMRW/). The trailing edge of MEMRW/ clocks U84-9 to its clear state, and DRDY goes false when the next DRCLK occurs. Thus, DRDY goes false while a byte is being serially shifted out of U89; after a byte has been shifted out, DRDY goes true to request the next byte.

Data being serially shifted out onto the TDATA line is at the same time being shifted onto the TXCRC DATA line to the input of the CRC generation logic. (Refer to sheet 7 of figure 6-2.) Before CRC generation begins, the Transmit CRC Preset (TXCRC PR/) signal, generated by flip-flop U92-5, is true, and consequently, because the output of AND-gate U75-6 is high, allows the CRC shift register to preload its contents with all ones. When the serial transfer on the TXCRC DATA line begins, the data bits are clocked by the 10-MHz SCLKED, least- significant bit first, through the CRC feedback shift register.

After transferring the last data byte, the DMA controller on the processor board asserts the End of Process (EOP/) signal. When EOP/ goes true, AND-gate U54-4 (5D5) is enabled and gates the BYTE CLOCK signal to the shutdown logic composed of flip-flops U53 and U52. During the first byte clock after EOP/ goes low, U69 multiplexes the last data word onto the TDATA line. On the leading edge of the second BYTE CLOCK after EOP/ becomes true, flip-flop U52-5 sets and applies a high input to the B select line, causing U69 to multiplex the ensuing FCS bit stream from the CRC generator onto the TDATA line. With both its A and B inputs high, U69 asserts the Check Word Enable (CWE) signal to the CRC generation logic. When CWE goes high, the CRC generator freezes the state of its feedback shift register and begins shifting out the complement of the computed 32-bit CRC field through Data Selector U69 onto the TDATA line.

5-6. MANCHESTER ENCODING

The serial data stream on the TDATA line is applied to the input of the Manchester encoder logic shown on sheet 2 of figure 6-2. The encoder translates 20-MHz clock OSC and TDATA into a single, phase-encoded, self-synchronizable serial bit stream. A typical serial bit stream waveform as seen on the Transmit Data (TXD) line and the transceiver cable is shown in figure 5-1.

The TDATA is translated to ECL level by differential amplifier U50 (2D7) and applied through NOR-gates U14-2 and U14-3 to the J-K inputs of flip-flop U32-15. The 20-MHz oscillator frequency, from which the 10-MHz bit clock (SCLK) is derived, is applied through U50-7 to clock flip-flop U32 (2D4). Referring to the timing diagram in figure 5-3, it can be seen that the purpose of the U32 is to ensure that the transition on the TXD line occurs in the middle of each bit cell.

As shown in figure 5-3, the data on the TDATA line must be valid at the beginning of the bit cell when OSC is high and SCLK is low. On the next rising edge

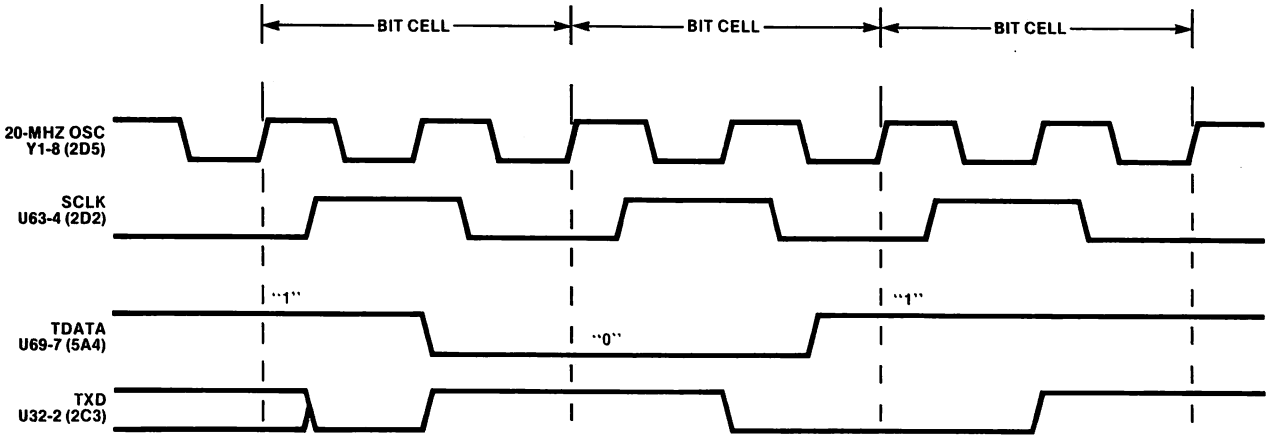


Figure 5-3. Manchester Encoding Timing 121746-20

of OSC, which occurs in the middle of the bit cell, flip-flop U32-15 latches the complement of the data present on its J-K inputs. The outputs of U32 are applied to the set and clear inputs of flip-flop U32 (2C3), which complements the latched data and drives the TXD line.

5-7. TRANSMIT SHUTDOWN

An orderly shutdown of the transmit logic is initiated in one of three ways: (1) normal shutdown when the DMA controller asserts the EOP/ signal, (2) transmit timeout due to an invalid frame size, and (3) a transmit collision occurs.

5-8. NORMAL SHUTDOWN. Four byte clocks occur during the time the CRC generator is shifting out the CRC field. On the rising edge of the fourth BYTE CLOCK/ after the DMA controller asserts EOP/, flip-flop U52-15 sets and (1) clears TXRQ flip-flop U33 and (2) inhibits AND-gate U19-4, which pulls the A select line low. Data Selector U69 is now in its shutdown state during which TDATA and CWE are low. Flip-flops U51, U53, and U92 are automatically cleared when TXRQ goes false, thus inhibiting the byte counter and clearing the CRC generator shift register. With TXRQ false, the rising edge of the next SCLK clocks ENABLE TXD flip-flop U91 to its clear state to disable the ECL transmitter.

5-9. TIMEOUT SHUTDOWN. One-shot U88 (2C7) is triggered at the beginning of the transmit sequence when TXRQ goes true. If the maximum frame size shown in figure 3-1 is exceeded, 5.2-millisecond one-shot U88 (2C7) times out and the trailing (rising edge) of the Transmit Time Out (XMT TO/) pulse clocks flip-flop U73 (5C5) to its set state. Pin 5 of U73 transmits the Transmit Time Out (TXTO) status bit to the processor board; pin 6 of U73 disables Data Selector U69 and, via AND-gate U66-8, generates an End of Processor (EOP/) signal to the DMA controller. Four byte clocks after EOP/ goes true, shutdown occurs as described in paragraph 5-8.

5-10. COLLISION SHUTDOWN. The user-supplied transceiver assembly must include a collision detector to sense when more than one station attempts simultaneous transmission. When the transceiver asserts the 10-MHz COLLISION/ signal, the output of AND-gate U54-10 (2B5) drives the

COLLLSION signal true to clock flip-flop U73 (5B5) to its set state. Pin 9 of U73 generates the Transmit Collision (TXCLSN) status to the processor board; pin 8 of U73, via OR-gate U74-11 and NAND-gate U66-8, generates an End of Process (EOP/) signal. The EOP/ signal, which is supplied to the DMA controller, also enables NAND-gate U72-6 (5BC) to generate a Transmit Complete (TXC/) interrupt to the processor board. In order to allow at least 32 bits and not more than 48 bits to be generated for collision enforcement, pin 8 of U73 enables OR-gate U74-11 to disable the 1Y output of Data Selector U69. During the following four byte clocks, 32 zero bits are transmitted before shutdown occurs as described in paragraph 5-8.

5-11. RECEIVE SEQUENCE

Receive data appearing on the RXD line is applied through differential line receiver U6 (8C6), the output of which is supplied through AND-gate U5-3 to the input of OR-gate U5-7. Because the Receive Enable (RXEN/) sequence control signal from the processor board is true (low), OR-gate U5-7 transfers the buffered RXD data onto the RX DATA line to the input of the Manchester Decoder.

5-12. MANCHESTER DECODING

The phase-encoded, self-synchronizable incoming data on the Receive Data (RXD) line is converted to TTL level and separated into a 10-MHz RCV CLK signal and a serial bit stream on the RCV DATA and RCV DATA D10 lines.

Incoming data on the RXD line is buffered and inverted by differential line receiver U6 (8C6) and driven onto the RX DATA/ line by gate U5-7 (8C4). (Refer to figure 5-4.) The data on the RXD DATA/ line is applied simultaneously to the D input of flip-flop U25 (6D5) and through delay line DL1, differential line receiver U6, and delay line DL2 to one input of exclusive OR-gate U24. The RX DATA/ DLY transitions out of DL2-10 to one input of exclusive OR-gate U24 are those transitions on the RX DATA/ line delayed 75 nanoseconds. The second input to U24 is the Q output of flip-flop U25, which is delayed 40 nanoseconds by delay line DL3. By examination of figure 5-4 it can be seen that these two signals are exclusive ORed to develop the ECL CLK signal, which clocks the RX DATA/ into flip-flop U25. The rising edge of ECL CLK occurs 75 nanoseconds after the middle of the previous bit cell, which is the optimum time to sample the data in that

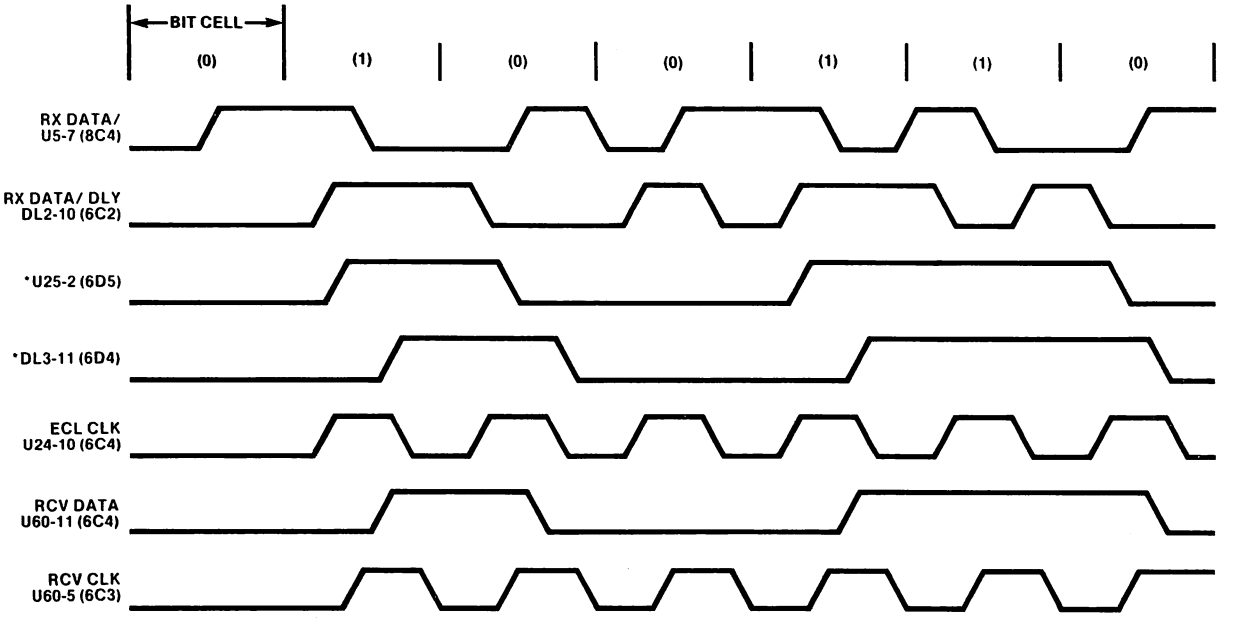


Figure 5-4. Manchester Decoding Timing

121746-21

cell. Valid data at the Q output of flip-flop U25 is applied through delay line DL3 and line receiver U60-11 to TTL level RCV DATA line. The RCV DATA is delayed 10 nanoseconds to produce RCV DATA D10.

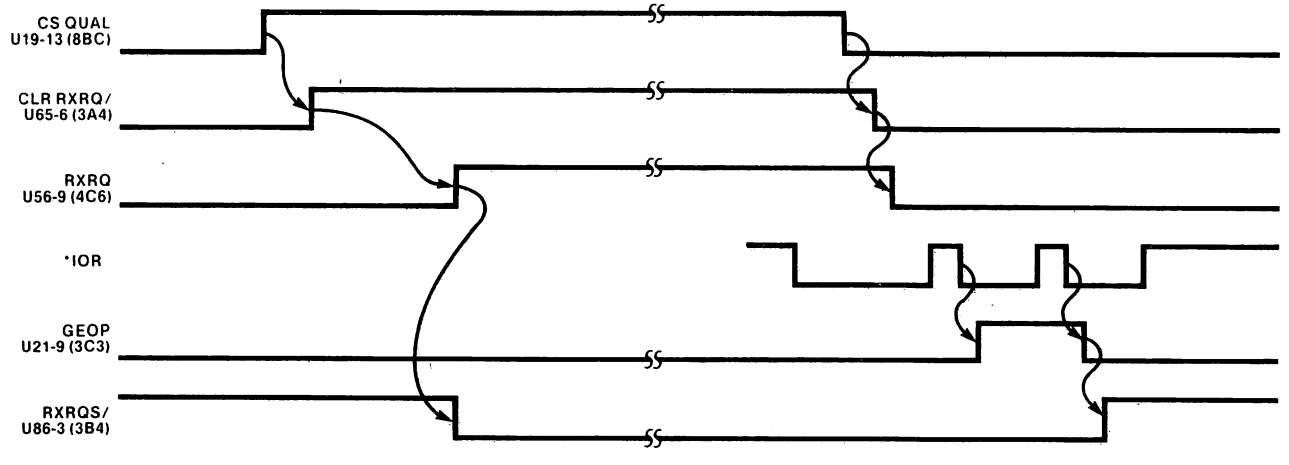
5-13. RECEIVE STARTUP

When the Read Address (READ ADD/) sequence control signal from the processor board is false (high), Data Selector U59 (4D6) selects and multiplexes RCV DATA D10 onto the MDATA line and RCV CLK onto the CS TRIGGER and MCLK lines. During periods of activity on the RXD line, CS TRIGGER repetitively triggers 300-nanosecond one-shot U11-13 (8B5) to generate Carrier Sense (CS) and, via NOR-gate U30-10, its complement CS/. The interpacket gap requirement is enforced by Timer U16 (5C7), which asserts the RCV LOCKOUT/ signal while CS/ is active low. When activity on the CS TRIGGER line ceases, one-shot U11-13 times out and releases the CS/ signal to allow U16 to be clocked by the toggling action of flip-flop U35. Thus, 9.6 microseconds after CS/ goes false, pin 6 of U16 goes high to release the RCV LOCKOUT/ signal. When RCV LOCKOUT/ is false, activity on the CS TRIGGER line allows the negative-going edge of CS/ to clock flip-flop U12 to its set state and, via AND-gate U19-3, generate the CS QUAL signal to enable Shift Register U78 (4B7) and initiate the receive startup. (Refer to figure 5-5.)

Shift Register U78, which is clocked on the rising edge of the 10-MHz clock SCLKED, generates Carrier Sense Delayed signals CSD1, CSD3, and CSD8. The CSD1 signal, which goes true 100-nanoseconds after CS QUAL goes high, inhibits NOR-gate U65-6 (3A4) to release the Clear Request (CLR RXRQ/) signal. The CSD3 signal goes true at the input of NAND-gate U55-8 300-nanoseconds after CS QUAL goes high. The CSD8 signal, which goes true 800 nanoseconds after CS QUAL goes high, clocks Receive Request (RXRQ) flip-flop U56-9 (4C6) to its set state. When RXRQ/ goes low, flip-flop U21-5 presets and enables NAND gate U86-3 to assert the Receive Request Synchronized (RXRQS/) signal to the processor board and initiate the DMA transfer. The clear side of the RXRQ flip-flop asserts the Receive CRC (RXCRC/) signal to Data Selector U62 (7B5). Data Selector U62, when RXCRC/ goes low, multiplexes the RCV CLK, RCV DATA, and CRC SYNC lines to the CRC generation logic.

5-14. ADDRESS RECOGNITION

The Address Equal (AD EQ) signal, depending on its status, determines whether or not the incoming data packet will be accepted and processed. The AD EQ signal will be asserted and allow the data packet to be accepted when (1) the incoming data packet contains a broadcast address, (2) the incoming data packet destination address matches the physical address stored in ROM, or (3) the PROMISCUOUS RCV/



*SIGNAL FROM PROCESSOR BOARD.

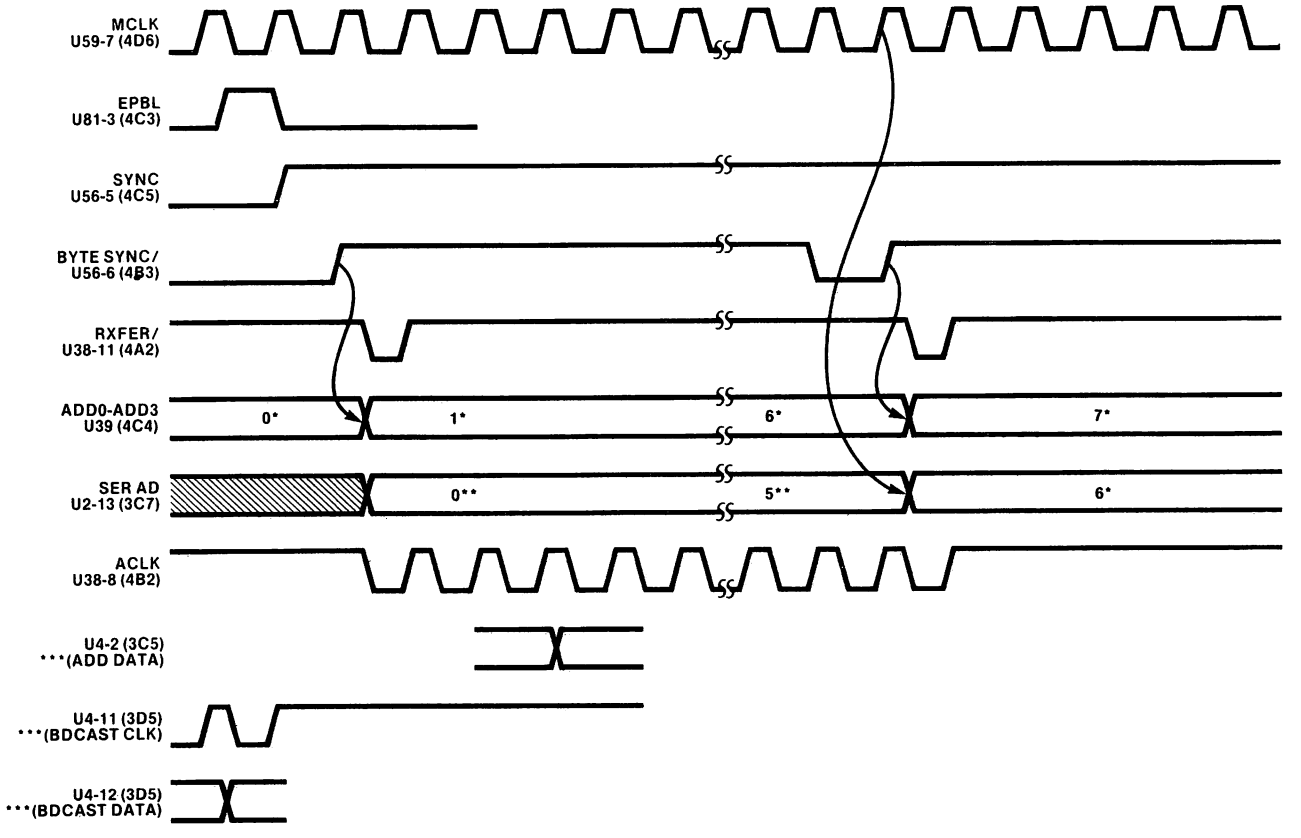
Figure 5-5. Receive Packet Framing Timing 121746-22

control bit from the processor board is true. When the PROMISCUOUS RCV/ bit is true, OR-gate U86-6 (3C4) asserts the AD EQ signal without regard to the destination address.

When RXRQ goes high, the multiplexed MCLK signal begins clocking in the serial bit stream on the MDATA line into Serial Data In (SDI) register U79/U80. The preamble consists of 62 bits of alternate ones and zeros followed by two consecutive ones. When U80-10 and U80-15 are set by the two consecutive ones at the end of the preamble, AND-gate U81-3 generates the End of Preamble (EPBL) signal. (Refer to figure 5-6.) With EPBL true, flip-flop U56-5 sets on the next rising edge of MCLK and asserts the SYNC signal to enable Binary Counter U39, Byte Clock Generator U37, and Address Clock U40-7. Byte Clock U37, which is clocked by the MCLK signal, generates the 800-nanosecond BYTE SYNC/ signal to synchronize the address generation logic composed of Binary Counter U39, Address ROM U1, and Shift Register U2. Byte Clock Generator U37 also synchronizes the transfer of data bytes from Serial Data In (SDI) register U79/U80.

After SYNC goes high, the next incoming data bit on the SDI0 line is the first (most-significant) bit of the destination address field. The first bit of the 48-bit destination address field distinguishes between a multicast (broadcast) address or a physical address. When the first bit is a one, indicating a broadcast address, SDI2 goes high and flip-flop U4-9 (3D5) sets on the next rising edge of MCLK. The clear side (pin 8) of U4, via NOR-gate U61-6 and OR-gate U86-6, generates the Address Equal (AD EQ) signal to enable reception of the remaining data packet.

When the first destination address bit is a zero, indicating a physical address, a bit-by-bit comparision of the destination address and the contents of



*HEX ADDRESS AT INPUT TO ROM U1.
**DATA BYTE AT OUTPUT OF ROM U1.
***SIGNALS IN PARENTHESES NOT SHOWN ON SCHEMATIC.

Figure 5-6. Address Recognition Timing 121746-23

Address ROM U1 is made to determine if an address match exists. Notice that before SYNC goes high, Binary Counter U39 is in its clear state and outputting all zeros on the ADD0-ADD3 lines to the input of Address ROM U1. While BYTE SYNC/ is high, the contents of data byte 0 (eight most-significant address bits) from U1 are loaded into Shift Register U2. When BYTE SYNC/ goes high, Binary Counter U39 increments the ROM address to U1 and U2 latches and begins shifting out the eight bits of the first byte to one of the two inputs of exclusive OR-gate U20-11. This sequence is repeated until U2 has loaded, latched, and shifted out the six address bytes (48 bits) contained in Address ROM U1.

The destination address field shifted out of U80-15 onto the SDI0 line and the address shifted out of U2 are applied to the inputs of exclusive OR-gate U20-11. The output of U20-11 will go low when the first address bit compares and will remain low as long as a bit-by-bit comparison of the remaining 47 bits exists. After the output of U20-11 goes low, flip-flop U4-5 is clocked to its clear state on the rising edge of the Address Clock (ACLK), which is generated by gating MCLK through NAND-gate U38-8 during address comparison. The clear side (pin 5) of U4-5, via NOR-gate U61-6 and OR-gate U86-6, asserts the AD EQ signal to enable the reception of the remaining data packet.

After six bytes of Address ROM U1 have been compared, Binary Counter U39 is clocked to the next sequential count (0110) and enables AND-gate U75-11 on the rising edge of the next BYTE SYNC. The output of U75-11 freezes the state of Binary Counter U39 and, on the next rising edge of MCLK, inhibits ACLK.

If any one of the physical address bits fails to match, the output of U20-11 goes high and flip-flop U4-5 sets and latches on the next rising edge of ACLK. Thus, AD EQ will go low and initiate a shutdown of the receive logic as described in paragraph 5-17.

5-15. DATA TRANSFER

Data bytes are transferred out of Serial Data In (SDI) register U79/U80 to a data buffer on the processor board at a 1.25-MHz rate. Byte Generator U37-2 goes high every 800 nanoseconds to generate the Receive Transfer (RXFER/) signal. The RXFER/ signal is inverted by U63-10 (6A3) to provide the Transfer (XFER) signal to clock the parallel byte on the SDI0-SDI7 lines into the processor board data buffer. The RXFER/ signal also clocks flip-flop U67-5 (6A6) to its set state, presetting U84-9. With U84-9 set, flip-flop U84-5 sets on the rising edge of the DRDY clock and asserts the Data Ready (DRDY) signal to the DMA controller. When DRDY goes true, the processor board transfers the data byte from the data buffer into memory and releases the MEMRW/ and IOR'/ signals. The positive-going edge of MEMRW/ clocks flip-flop U84-9 (6B4) to its clear state, allowing DRDY flip-flop U84-5 to be cleared on the next Data Ready Clock (DRCLK) from the processor board.

The next and succeeding data bytes are transferred at 800-nanosecond intervals from the SDI register to the processor as described above until a shutdown occurs as a result of Carrier Sense (CS/) going inactive or the DMA controller asserts the End of Process (EOP/) signal if the data packet length is exceeded.

5-16. RECEIVE SHUTDOWN

An orderly shutdown of the receive logic is initiated in one of three ways: (1) no address match condition occurs, (2) normal shutdown as a result of Carrier Sense (CS/) going inactive, or (3) the DMA controller detects a length error.

5-17. ADDRESS MISMATCH SHUTDOWN. If an address mismatch occurs, the AD EQ signal will go false and initiate a premature shutdown of the receive logic. When AD EQ goes false, NOR-gate U65-6 asserts the Clear Receive Request (CLR RXRQ/) signal to clear RXRQ flip-flop U56-9. Pin 9 of U56 goes low and clears the SDI register. The DMA controller reads two bytes of all zeros in the same manner as described in paragraph 5-15 before shutdown occurs.

On the trailing edge of the first IOR'/ signal from the DMA controller, flip-flop U21-9 is clocked to its set state and asserts the Gated End of Process (GEOP) signal. Thus, when GEOP goes high while AD EQ is low, NAND-gate U66-3 is enabled and asserts the End Of Process (EOP/) signal to auto-initialize the participating DMA controller receive channel. The trailing edge of the next (and final) IOR'/ signal clocks flip-flop U21-9, which (1) pulls GEOP low and (2) clocks flip-flop U21-5 to its clear state. Pin 5 of U21 clears flip-flop U4-5 and, via NAND-gate U83-3, releases the RXRQS/ signal.

5-18. NORMAL SHUTDOWN. When activity ceases on the CS TRIGGER line, on-shot U11-13 (8B5) times out and deactivates the CS and CS/ signals. The CS/ signal activates Timer U16 for inter-packet gap enforcement and inhibits NAND-gate U19-13 in order to deactivate the CS QUAL signal. After CS QUAL goes low, CSD1 goes low and enables NOR-gate U65-6 to assert the Clear Receive Request (CLR RXRQ/) signal, which clears RXRQ

flip-flop U56-9. The following occurs as a result of clearing the RXRQ flip-flop: (1) SDI register U79/U80 is cleared, (2) the RXRQ/ signal goes high, (3) and CRC ERR flip-flop U82-5 is clocked. If the ERR signal generated by the CRC generator is true, indicating that the received packet contains a CRC error, U82-5 goes set and transmits the CRC ERR status to the processor.

With the SDI register in its clear state, two invalid bytes are transferred to the processor board during normal shutdown. The RXRQ/ signal, when high, releases the preset input of flip-flop U21-5. On the trailing edge of the next to last IOR'/ signal from the DMA controller, flip-flop U21-9 is clocked to its set state and asserts the GEOP signal. If the CRC feedback register has verified that no CRC error exists, the GEOP signal (1) enables NAND-gate to generate Receive Complete (RXCMP) signal and interrupt the processor. The trailing edge of the final IOR'/ signal clocks flip-flop U21-9, which (1) pulls GEOP low and clocks flip-flop U21-5 to its clear state. (When RX CMP goes low, the DMA channel select logic rotates to select the next sequential DMA receive channel for the next incoming data packet.) Pin 5 of U21 clears flip-flop U4-5 and, via NAND-gate U83-3, releases the RXRQS/ signal.

If a CRC error is computed in the CRC feedback register when CS QUAL goes inactive, NAND-gate U26-8 (7D3) will be inhibited and assert the Error (ERR) signal. The ERR signal allows flip-flop U82-9 to be set on the trailing edge of CSD3. Pin 9 of U82 transmits the CRC ERR status to the processor and pin 8, via OR-gate U55-11, asserts the Receive Error (RXER) signal. The RXER signal enables AND-gate and inhibits NAND-gate U77-8. Thus, when a packet contains a CRC error during normal mode operation, the EOP/ signal will be asserted to autoinitialize the participating DMA controller receive channel; however, the RX CMP signal will not be generated to interrupt the processor, and no rotation of the DMA controller receive channel occurs.

5-19. LENGTH ERROR SHUTDOWN. The Base Word Count register in each DMA controller receive channel is initialized with a count of 1521, which is the maximum allowable number of bytes to be transferred without generating a length error. When the Current Word Count register of the participating receive channel decrements to zero, the DMA controller asserts the EOP/ signal to initiate a shutdown. The EOP signal enables NAND-gate U72-3, the output of which (1) presets GEOP flip-flop U21-9 and (2) enables AND-NOR gate U85-6. When enabled, the output of U85-6 asserts LEN DATA/ and, via NOR-gate U65-6, CLR RXRQ/. The CLR RXRQ/ signal clears RXRQ flip-flop U56-9, which (1) clears the SDI register and (2) clocks LEN ERR flip-flop U82-5 to its clear state, asserting the LEN ERR and RXER signals, and (3) clocks CRC ERR flip-flop U82-9 to its set state. (Flip-flop U82-9 sets because the ERR signal, generated by NAND-gate U26-8 in the CRC generator error detection logic, is false.) The RXER signal (1) inhibits NAND-gate U77-8 to prevent the Receive Complete (RXCMP) from going true and interrupting the processor and (2) enables AND-gate U30-13 to generate the ERROR signal.

After asserting EOP/ and releasing IOR'/, the DMA controller releases Hold Request (HREQ), which causes the Hold Acknowledge (HLDA) to go low after the processor board DMA bus is released. The negative-going edge of HLDA, via AND-NOR gate U85-8, clocks GEOP flip-flop U21-9 to its clear state. Pin 5 of U21 clears flip-flop U4-5 and, via NAND-gate U83-3, releases the RXRQS/ signal. The CRC ERR and LEN ERR flip-flops are cleared by the RESET ERROR/ signal from the processor board.

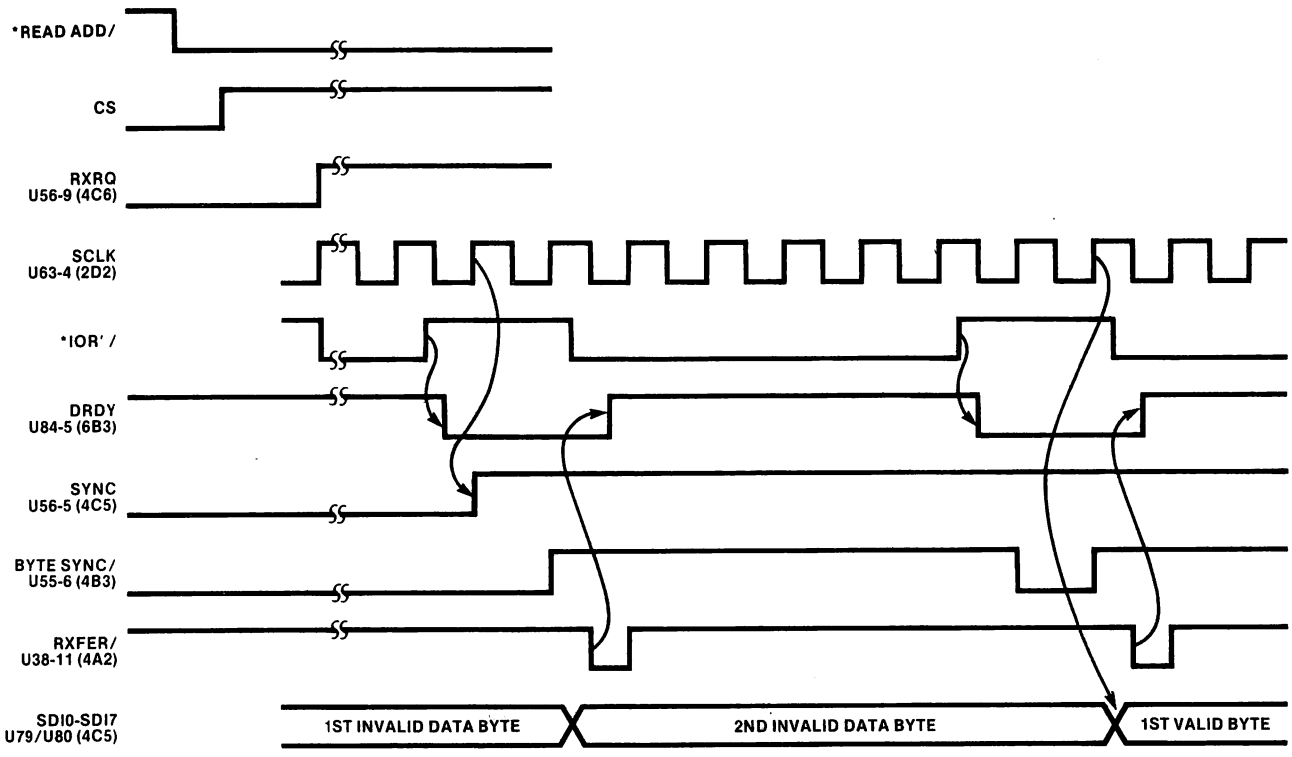
5-20. READ ADDRESS SEQUENCE

The read address sequence reads the physical address stored in Address ROM U1 and stores this address in SRAM memory on the processor board.

5-21. READ ADDRESS STARTUP

THe processor board must disable the Receive Enable (RXEN) signal at least 12 microseconds before asserting the Read Address (READ ADD/) control signal. When READ ADD/ goes true (low), Data Selector U59 (4D6) selects and multiplexes the SCLKED signal onto the CS TRIGGER line, the SCLK signal onto the MCLK line, and the DRDY/ signal to the Q input of flip-flop U56-5. (Refer to figure 5-7.) The CS TRIGGER repetitively triggers one-shot U11-13 (8B5) to generate Carrier Sense (CS) and its complement CS/. The negative-going edge of CS/ clocks flip-flop U12 to its set state to enable AND-gate U19-3 and generate the CS QUAL signal and initiate the read address startup.

As described in paragraph 5-13, Shift Register U78 (4BC) generates CSD1, CSD3, and CSD8 after CS QUAL goes true. After CS QUAL goes true, CSD1 goes high and inhibits NOR-gate U65-6 to release the Clear Receive Request (CLR RXRQ/) signal; CSD3 goes high at the input of NAND-gate U55-8; and CSD8 goes high and clocks Receive Request (RXRQ) flip-flop U56 (4C6) to its set state, asserting the RXRQ and, via NAND-gate U55-3, the RXRQ/ signals. The RXRQ signal enables Serial Data In (SDI) register U79/U8. The RXRQ/ signal presets



*SIGNAL FROM PROCESSOR BOARD

Figure 5-7. Read Address Startup Timing 121746-24

flip-flop U21-5 (3C4), which enables NAND-gate U86-3 to assert the Receive Request Synchronized (RXRQS/) signal to the DMA controller on the processor board, initiating the DMA transfer.

5-22. ADDRESS TRANSFER

After gaining control of the DMA bus, the DMA controller pulls I/O Read (IOR'/) and Memory Read Write (MEMRW/) low and reads the first of two invalid data bytes. Flip-flop U84-9 (6B4) is clocked to its clear state on the trailing edge of MEMRW/ and, on the rising edge of the following Data Read Clock (DRCLK), the Data Ready (DRDY) signal to the processor board goes low and the DRDY/ signal to the Q input of flip-flop U56-5 (4C6) goes high. The rising edge of the following SCLK signal clocks flip-flop U56-5 to its set state and asserts the SYNC signal, which enables Binary Counter U39, Byte Clock Generator U37, and Address Clock U40-7. Byte Clock Generator U37, which is clocked by the SCLK signal multiplexed onto the MCLK line, generates the 100-nanosecond BYTE SYNC/ signal every 800 nanoseconds. The BYTE SYNC/ signal synchronizes the address generation logic composed of Binary Counter U39, Address ROM U1, and Shift Register U2. Shift Register U2 loads a parallel address byte from Address ROM U1 when BYTE SYNC/ is true, and latches the data byte and begins shifting it into the SDI register when BYTE SYNC/ goes false. Binary Counter U39 increments the address on the ADD0-ADD3 lines to Address ROM U1 each time BYTE SYNC/ makes a low-to-high transition; 50 nanoseconds later, NAND-gate U38-11 is enabled and generates the Receive Transfer (RXFER/) signal.

Before SYNC goes high, Byte Clock Generator U37 is disabled and Binary Counter U39 is in its clear state and outputting all zeros on the ADD0-ADD3

lines to Address ROM U1. On the rising edge of the first SCLK after SYNC goes high, BYTE SYNC/ goes false. On the rising edge of BYTE SYNC/, Shift Register U2 latches the first address byte and begins shifting it into the SDI register. On the falling edge of SCLK after BYTE SYNC/ goes false, NAND-gate U38-11 is enabled and pulls RXFER/ low. The RXFER signal is inverted by U63-100 (6A3) to (1) provide the Transfer (XFER) signal to clock the contents of the SDI register into the processor board data buffer and (2) clock flip-flop U67-5 (6A6) to its set state and, via flip-flops U67-5, U84-9, and U84-5, generate the Data Ready (DRDY) signal. Since Shift Register U2 has not completed shifting the first valid address byte into the SDI register, the second of two invalid bytes are read by the DMA controller when the next IOR'/ and MEMRW/ signals are asserted.

The first address byte, which is valid in the SDI register when the ensuing BYTE SYNC/ signal goes true, and subsequent address bytes are transferred at 800-nanosecond intervals in the same manner as described above until the DMA controller asserts the End of Process (EOP/) signal.

5-23. READ ADDRESS SHUTDOWN

Before issuing the READ ADD/ control signal, the Base Word Count register in the participating DMA controller receive channel is initialized with a count of 18 (2 invalid bytes plus 16-byte contents of Address ROM U1). When the Current Address Register of the participating receive channel decrements to zero, the DMA controller asserts the EOP/ signal to initiate a shutdown. The EOP/ signal, via NAND-gate U72-3, enables AND-OR-gate U85-6 which (1) asserts the LEN DATA/ signal and (2) enables NOR-gate U65-6 to pull CLR RXRQ/ low and clear RXRQ flip-flop U56-9. Pin 9 of U56 goes low and (1) clears the SDI register, (2) pulls RXRQ low, and (3) releases RXRQ/. Pin 8 of U56 goes high and clocks LEN ERR/ flip-flop U82-5 to its clear state and assert LEN ERR/ and the processor LEN ERR status. The LEN ERR/ signal, via OR-gate U55-11, also generates the RXER signal.

After asserting EOP/, the DMA controller will not accept any further data and therefore IOR/ remains false, Thus, with LEN ERR time and IOR/ false, the rising edge of the 5-MHz clock enables AND-NOR-gate U85-8 to clock flip-flop U21-9 to its set state and asserts GEOP. (Notice that because RXER is high, U77-8 is inhibited and prevents RX CMP from going true and interrupting the processor. The second 5-MHz clock after LEN ERR goes true clocks U21-9 to its clear state, pulling GEOP low and clocking flip-flop U21-5 to its clear state. Pin 5 of U21 clears flip-flop U4-5 and, via NAND-gate U83-3, releases the RXRQS/ signal.

After the Read Address sequence is complete, the processor board first clears the READ ADD/ control bit and sets the CLR SER control bit, and then clears the CLR SER control bit.

5-24. VERIFY SERDES SEQUENCE

The verify SerDes sequence transmits packets, with good and bad CRC data, to broadcast and non-broadcast destination addresses. This sequence is the same as a transmit sequence and a receive sequence operating simultaneously except that the FCS field is not computed during the transmit sequence and the receive data is not stored in SRAM memory. Verification of the successful transmit and receive functions is accomplished as in a normal receive sequence by checking the FCS field in the transmit packet. Successful execution of this test is verified by the LEN ERR and CRC ERR status bits.

The verify transmit packet is transmitted as in a normal transmit sequence; however, the line receiver logic is disabled because AND-gate U5-3 (8C5) is inhibited by the VERIFY ON BRD signal. Because AND-gate U14-14 (2C2) is enabled, the output of the Manchester Encoder at flip-flop U32-14 (2C4) is looped back to the input of the Manchester Decoder.

5-25. VERIFY TRANSCEIVER SEQUENCE

The verify transceiver sequence is the same as the verify SerDes sequence except the line receiver logic is enabled and the transmit packet is echoed back from the transceiver to the enabled line receiver logic.

CHAPTER 6
SERVICE INFORMATION

6-1. INTRODUCTION

This chapter provides service and repair assistance instructions, service diagrams, a parts list for each printed circuit board assembly, and a description of the firmware-based confidence test.

6.2 SERVICE DIAGRAMS

The controller schematic diagrams are provided in figures 6-1 and 6-2. Note that these diagrams are intended only for reference and reflect the iSBC 550 Ethernet Communications Controller design level only at the time this manual was printed. The schematic diagrams packaged with the controller reflect the current design level and, when not identical to the corresponding diagrams in the manual, supersede the diagrams herein.

6-3. SERVICE AND REPAIR ASSISTANCE

The best service for your Intel product will be provided by an Intel Customer Engineer. These trained professionals will provide prompt, efficient on-site installation, preventive maintenance, and corrective maintenance services that will keep your equipment in the best possible operating condition.

Your Intel Customer Engineer can provide the service you need through a prepaid service contract or on an hourly charge basis. For further information, contact your local Intel office.

When it is impossible for you to use the services of an Intel Customer Engineer or when Intel service is not available in your local area, you may contact the Intel Service Center directly at one of the following numbers:

Telephone:

From Alaska, Arizona, or Hawaii call—
(602) 869-4600

From all other U.S. locations call toll free—
(800) 528-0595

TWX: 910-951-1330

Never return equipment to Intel for service or repair before you contact an Intel Customer Engineer or the Intel Service Center.

If return of your equipment is necessary, you will be given a Repair Authorization Number, shipping instructions, and other important information that will help Intel provide you with fast, efficient service. If the product is being returned because of damage sustained during shipment, or if the product is out of warranty, a purchase order is necessary in order for the Intel Service Center to make the repair.

When preparing the product for shipment to the Service Center, use the original factory packaging material if available. If the original packaging is not available, wrap the product in a cushioning material such as Air Cap SD-240, manufactured by the Sealed Air Corporation, Hawthorne, N.J. (or equivalent) and enclose in a heavy-duty corrugated shipping carton. Seal the carton securely, mark it "FRAGILE" to ensure careful handling, and ship it to the address specified by the Intel Service Center.

NOTE

Customers outside of the United States should contact their sales source (Intel Sales Office or Authorized Intel Distributor) for directions on obtaining service or repair assistance.

6-4. CONFIDENCE TEST

The firmware-based confidence test executes once on power-up and each time the host system is reset. This test can optionally be forced to loop repeatedly by installing a plug-in jumper in position E22-E23. (See figure 2-3.) The confidence test includes 20 individual tests that exercise all the processor board on-board memory and programmable LSI chips, and the SerDes on-board PROM containing the station address. The test also checks the controller's ability to perform the following functions:

a. Transmit a data packet with proper CRC field.

b. Receive a data packet in broadcast and non-broadcast modes.

c. Detect good and bad CRC fields in receive data packets.

The LED on the processor board will light and remain lighted if any one of the 20 individual tests fails.

6-5. REPLACEABLE COMPONENTS

This section contains the information necessary for the procurement of replacement components directly from commercial sources. Component manufacturers have been abbreviated in the parts list with either a two, three or four character code. Table 6-1 cross-references the manufacturer's code with the name and location of the prime commerical source. Tables 6-2 and 6-3, respectively, are the lists of replaceable components for the processor board and SerDes board. Note that components that are available commercially are listed in the "MFR CODE" column as "COML" and that they are ordered by description (OBD). Every effort should be made to procure commercially-available components from a local distributor.

Table 6-1. List of Manufacturer's Codes

Mfr. Code	Manufacturer	Address	Mfr. Code	Manufacturer	Address
AMP	AMP, Inc.	Harrisburg, PA	MOT	Motorola Semiconductor	Phoenix, AZ
AUG	AUGAT, Inc.	Attleboro, MA	NATL	National Semiconductor	Sunnyvale, CA
BECK	Beckman Instruments	Fullerton, CA	PCA	PCA Electronics	Sepulveda, CA
BOUR	Bourns, Inc.	Riverside, CA	SIG	Signetics Corp.	Sunnyvale, CA
BURN	Burndy	Norwalk, CT	SPEC	Spectral Dynamics	San Diego, CA
CRYS	Crystek Crystals, Inc.	Ft. Myers, FL	SPRG	Sprague Electric	Longwood, FL
DIAL	Dialight Corp.	Brooklyn, NY	TI	Texas Instruments	Dallas, TX
INTEL	Intel Corp.	Santa Clara, CA	COML	Available from any commerical source; order by description (OBD).	

Table 6-2. Processor Board Replaceable Parts List

Reference Designation	Description	Mfr. Part No.	Mfr. Code	Qty.
CR1	Diode, 1N4148	OBD	COML	1
C1-13,15-18,20-36, 38-58,60-63,65-70, 72-88,90-99	Cap., ceramic, 0.1 μF	OBD	COML	92
C14,19,37,59,102	Cap., tantalum, 2.2 μF, 20 VDCW, 10%	OBD	COML	5
C64	Cap., ceramic, 1000 pF	OBD	COML	1
C89	Cap., tantalum, 10 μF, 20 VDCW, 10%	OBD	COML	1
C100	Cap., tantalum, 22 μF, 15 VDCW, 10%	OBD	COML	1
C101	Cap., tantalum, 6.8 μF, 35 VDCW, 20%	OBD	COML	1
DS1	Diode, LED, R/A, red	550-2206	DIAL	1
Q1	Transistor, 2N2222	OBD	COML	1
RP1	Res., pack, 15R, 16-pin, 10k	898-1-R10K	BECK	1
RP2,4	Res., pack, 15R, 16-pin, 2.2k	898-1-R2.2K	BECK	2
RP3	Res., pack, 9R, 10-pin, 10k	785-1-R10K	BECK	1
RP5	Res., pack, 5R, 6-pin, 10k	4306R-101-103	BOUR	1
R1	Res., fxd, carbon, 1k, ¼W, 5%	OBD	COML	1
R2-4,6-10,15,16, 18-23,25,28,30,31	Res., fxd, carbon, 2.2k, ¼W, 5*	OBD	COML	20
R5	Res., fxd, carbon, 120, ¼W, 5%	OBD	COML	1
R11,17,29	Res., fxd, carbon, 470, ¼W, 5%	OBD	COML	3
R12,14	Res., fxd, carbon, 10k, ¼W, 5%	OBD	COML	2
R13	Res., fxd, carbon, 330k, ¼W, 5%	OBD	COML	1
R24	Res., fxd, carbon, 22k, ¼W, 5%	OBD	COML	1
R26	Res., fxd, carbon, 330, ¼W, 5%	OBD	COML	1
R27	Res., fxd, carbon, 220, ¼W, 5%	OBD	COML	1
R32,33	Res., fxd, carbon, 510, ¼W, 5%	OBD	COML	2

Table 6-2. Processor Board Replaceable Parts List (Cont'd.)

Reference Designation	Description	Mfr. Part No.	Mfr. Code	Qty.
S1	Switch, 9 position	87-21-19	SPEC	1
U3	IC, dual 4-input NAND-gates	74S20	TI	1
U4	IC, triple 3-input NAND-gates	74S10	TI	1
U5-12	IC, Intel 2118-4 16k Dynamic RAM	2118-4	COML	8
U13	IC, Intel 8202A Dynamic RAM Controller	8202A	COML	1
U14	IC, triple 3-input NOR-gates	74LS27	TI	1
U15,48,93	IC, hex inverters	74LS04	TI	3
U17	IC, 3-to-8 line decoder/multiplexer	74LS138	TI	1
U18	IC, quad S/R latches	74LS279	TI	1
U19,26	IC, quad 2-input NAND-gates	74LS00	TI	2
U20-23,39-42,61-64, 78-81	IC, Intel 2114AL-3 4k Static RAM	2114AL-3	COML	16
U25,86	IC, quad 2-input OR-gates	74LS32	TI	2
U27,36,51,69	IC, dual D-type flip-flops	74LS74A	TI	4
U28	IC, quad 2-input NOR-gates	74S02	TI	1
U29,82	IC, quad 2-input NAND-gates	74S00	TI	2
U30	IC, memory decoder PROM	104597-001	INTEL	1
U32,57	IC, 8-bit bidirectional receiver	8304	NATL	2
U33,53,55,56,71, 72,77	IC, octal D-type latches	74LS373	TI	7
U34	IC, dual 2-to-4 decoder/multiplexers	74S139	TI	1
U35	IC, quad 2-input OR-gates	74S32	TI	1
U37,83	IC, quad D-type flip-flops	74LS175	TI	2
U38	IC, Intel 8237-2 Prog. DMA Controller	8237-2	COML	1
U43,96	IC, quad 2-input AND-gates	74LS08	TI	2
U44,49,60	IC, quad 2-input NOR-gates	74LS02	TI	3
U45	IC, triple 3-input AND-gates	74LS11	TI	1
U46	IC, dual J-K flip-flops	74S112	TI	1
U47	IC, 4-bit parallel shift register	74195	TI	1
U50	IC, hex drivers	74368A	TI	1
U52,88,89	IC, Intel 8283 Octal Latch	8283	COML	3
U54	IC, Intel 8088 8-Bit Microprocessor	8088	COML	1
U58	IC, 32k PROM	104598-001	INTEL	1
U59	IC, 32k PROM	104599-001	INTEL	1
U65	IC, dual monostable multivibrators	74123	TI	1
U66	IC, quad 3-state bus buffer gates	74LS125	TI	1
U67	IC, quad D-type flip-flops	74S74	TI	1
U68	IC, hex inverters	74S04	TI	1
U70	IC, Intel 8284A Clock Generator/Driver	8284A	COML	1
U73,85	IC, Intel 8288 Bus Controller	8288	COML	2
U74	IC, octal buffers/drivers/receivers	74S241	TI	1
U75	IC, Intel 8253 Prog. Interval TImer	8253	COML	1
U76	IC, Intel 8259A Prog. Interrupt Controller	8259A	COML	1
U84	IC, Intel 8289 Bus Arbiter	8289	COML	1
U87,90	IC, I/O decoder PROM	104596-001	INTEL	2
U91	IC, Intel 8287 Octal Bus Transceiver	8287	COML	1
U92	IC, Intel 8255A Prog. Peripheral Interface	8255A	COML	1
U94	IC, octal D-type flip-flops	74S374	TI	1
U95	IC, octal D-type flip-flops	74LS374	TI	1
U97	IC, 3-to-8 line decoder/multiplexer	74S138	TI	1
XU13,38	Socket, IC, 40-pin	DILB40P-108	BURN	2
XU30,87,90	Socket, IC, 18-pin	DILB18P-108	BURN	3
XU54	Socket, IC, 40-pin	540-AG11D	AUG	1
XU58,59	Socket, IC, 24-pin	524-AG11D	AUG	2
XU76	Socket, IC, 28-pin	DILB-28P-108	BURN	1
Y1	Crystal, 20.000 MHz	K1115A-20MHz	MOT	1
Y2	Crystal, 15.000 MHz	M22B	CRYS	

Table 6-3. SerDes Board Replaceable Parts List

Reference Designation	Description	Mfr. Part No.	Mfr. Code	Qty.
C1-9,11-28,30-80	Cap., ceramic, 0.1 μF	OBD	COML	78
C10,29	Cap., mica, 68 pF, 5%	OBD	COML	2
C81,82	Cap., ceramic, axial, 0.1 μF	OBD	COML	2
C83	Cap., tantalum, 22 μF, 20 VDCW, 10%	OBD	COML	1
C84	Cap., ceramic, axial, 0.33 μF	OBD	COML	1
DL1,3	Delay Line, 50 ns	EP 19824	PCA	2
DL2	Delay Line, 30 ns	60Z1122	SPRG	1
J3	Connector, HDR, R/A, 10P	87516-1	AMP	1
RP1	Res., pack, 8-pin, 7 x 510	764-1-R510	BECK	1
RP2	Res., pack, 10-pin, 9 x 1k	761-1-R1K	BECK	1
RP3	Res., pack, 8-pin, 7 x 10k	764-1-R10K	BECK	1
R1,2,23-25,30,35, 36,40,55-57,60, 62,63,65-68,71, 73-75,77,78,82	Res., fxd, carbon, 2.2k, ¼W, 5%	OBD	COML	26
R3,5-9	Res., fxd, carbon, 390, ¼W, 5%	OBD	COML	6
R4,10,11	Res., fxd, carbon, 1.8k, ¼W, 5%	OBD	COML	3
R12,13,17,18	Res., fxd, carbon, 39, ¼W, 5%	OBD	COML	4
R14,15,29,37,38, 43,46,58,59	Res., fxd, carbon, 510, ¼W, 5%	OBD	COML	9
R16,39,51,52	Res., fxd, carbon, 180, ¼W, 5%	OBD	COML	4
R19,22,50,53, 79,80	Res., fxd, carbon, 270, ¼W, 5%	OBD	COML	6
R20,21,49,54	Res., fxd, carbon, 820, ¼W, 5%	OBD	COML	4
R27,41,48	Res., fxd, carbon, 240, ¼W, 5*	OBD	COML	3
R28,42	Res., fxd, carbon, 160, ¼W, 5%	OBD	COML	2
R32,34	Res., fxd, carbon, 10k, ¼W, 5%	OBD	COML	2
R44	Res., fxd, carbon, 82, ¼W, 5%	OBD	COML	1
R45,61	Res., fxd, carbon, 120, ¼W, 5%	OBD	COML	2
R47,76	Res., fxd, carbon, 10k, ¼W, 5%	OBD	COML	2
R64	Res., fxd, carbon, 3K, ¼W, 5%	OBD	COML	1
R70	Res., fxd, carbon, 47k, ¼W, 5%	OBD	COML	1
R81	Res., fxd, carbon, 1k, ¼W, 5%	OBD	COML	1
**U1	IC, Ethernet address PROM	**	—	1
U2,89	IC, 8-bit shift register	74166	TI	2
U3,49,58,87	IC, hex inverters	74LS04	TI	4
U4,17,33,70,83, 84,90,91,92	IC, dual D-type flip-flops	74S74	TI	9
*U5	IC, triple 2-3-2 input OR/NOR gate	10105	SIG	1
*U6,13,50	IC, triple differential line receiver	10116	SIG	3
U7,27	IC, dual 5-input NOR-gates	74S260	TI	2
U8,9,45,46,51	IC, octal D-type flip-flops	74LS273	TI	5
U10,30,54	IC, quad 2-input NOR-gates	74LS02	TI	3
U11,88	IC, dual monostable multivibrators	74123	TI	2
U12	IC, dual J-K flip-flops	74LS112	TI	1
*U14	IC, quad 2-input NOR-gates	10102	SIG	1
U15,38	IC, quad 2-input OR-gates	74S32	TI	2
U16	IC, 8-bit parallel output shift register	74LS164	TI	1
U19	IC, quad 2-input NOR-gates	74S02	TI	1
U20,29,44,47,64	IC, quad 2-input exclusive OR-gates	74S86	TI	5
U21,35,53,56,73, 82,93	IC, quad D-type flip-flops	74LS74	TI	7
U22	IC, triple 3-input AND-gates	74LS11	TI	1
*U24	IC, triple exclusive OR-gates	10107	SIG	1
*U25	IC, quad D-type flip-flops	10131	SIG	1
U26	IC, 8-input NAND-gate	74S30	TI	1
U28	IC, 13-input NAND-gate	74S133	TI	1
U31,60	IC, quad 2-input OR-gates	26LS32	TI	2
*U32	ICE, dual J-K flip-flops	10135	SIG	1
U34,61,81	IC, quad 2-input AND-gates	74LS08	TI	3

Table 6-3. SerDes Board Replaceable Parts List (Cont'd.)

Reference Designation	Description	Mfr. Part No.	Mfr. Code	Qty.
U36,37,79,80	IC, quad D-type flip-flops	74S175	TI	4
U39	IC, synchronous binary 4-bit counter	74LS161	TI	1
U40,67	IC, dual J-K flip-flops	74S112	TI	2
U43,55,74,76,86	IC, quad 2-input NAND-gates	74LS00	TI	5
U48	IC, triple 3-input NAND-gates	74LS10	TI	1
U52	IC, hex D-type flip-flops	74S174	TI	1
U57,72	IC, quad 2-input OR-gates	74LS32	TI	2
U59,62	IC, quad 2-to-1 data selector/mux	74LS157	TI	2
U63	IC, hex inverters	74S04	TI	1
U65	IC, dual 4-input AND-gates	74LS21	TI	1
U66	IC, quad 2-input NAND-gates	7438	TI	1
U68	IC, triple 3-input NAND gates	74S10	TI	1
U69	IC, quad 4-to-1 data selector/mux	74S153	TI	1
U71	IC, quad 2-input AND-gates	74S08	TI	1
U75	IC, quad 2-input NAND-gates	74S00	TI	1
U77	IC, dual 4-input NAND-gates	74LS40	TI	1
U78	IC, 8-bit parallel output shift register	74164	TI	1
U85	IC, dual AND-OR invert gates	7451	TI	1
Y1	Crystal, 20.000 MHz	K1115A-20MHz	MOT	1

*These IC's are ECL type. All other IC's are TTL type.
**Board must be returned to Intel for U1 replacement.